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Most Young Scholars Grant (Columbus Program) :A Dopingless Transistor

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By adopting the charge-plasma concept, dopingless FETs with metal-semiconductor (MS) and metal-insulator- semiconductor (MIS) contacts in parallel at the source/drain (SD) have been studied in this work. It is found that currents may be mainly pathing through the MIS contacts for a given SD metal workfunction when the insulator thickness is thin enough. In order to avoid the potential penalty caused by Fermi level pinning, the dopingless FET with merely SD MIS contacts has been proposed as well. The impacts of insulator material parameters on the electrical characteristics of the dopingless FET, such as bandgap, electron affinity, dielectric constant and physical thickness, have been investigated systematically. Based on numerical simulations, this work provides a general guideline with physical insights for designing dopingless FETs with high-permittivity insulator at the SD MIS contacts.

The proposed device (Fig. 1) with an active dopingless Si surrounded entirely by thin insulators features merely MIS contacts at SD, and which can be formed precisely by the atomic layer deposition in real process. Two adjustable metal workfunction at SD (WF_{SD}) and gate (WF_G) are specified in simulations. The gate electrode is isolated from SD by a distance of 5 nm, and which can be achieved by the spacer formation in real process. Variable Si body thickness T and insulator thickness t are used to investigate their impacts on the electrical characteristics of the devices. To mimic the reality, the Si background doping concentration is specified at 1×10^{15} cm^{-3}, instead of the theoretical value of 1×10^{10} cm^{-3} at room temperature. Note that all results show in this work would not be changed obviously by the background doping ranging from 1×10^{10} to 1×10^{17} cm^{-3}.

The electrical characteristics are computed by solving the Poisson and continuity equations self-consistently involving a quantum correction model to consider the carrier redistribution near the insulator interface. Physical models include nonlocal band-to-band tunneling and nonlocal tunneling through insulating and Schottky barriers. The tunneling probability of the nonlocal tunneling models is calculated based on the WKB (Wentzel-Kramers-Brillouin) approximation of the electron wavefunction. Note that the gate tunneling leakage current has been excluded in simulations because it can be a valid assumption when a high-k metal gate stack is employed in real process. Phonon-limited bulk carrier mobility, carrier velocity saturation and Shockley-Read-Hall generation are considered as well.

Though MIGS is not considered directly, its consequence, namely effective WF_{SD} due to FLP, is a variable in simulations. With this approach, the electrical performance of the device in Fig. 1 will be enhanced when the workfunction is depinned and approaching to an ideal value, such as low WF_{SD} ~ 4.0 eV for n-channel. Note that Si electron affinity χ_e = 4.05 eV, dielectric constant ε = 11.9 and E_g = 1.12 eV are specified in all simulations.

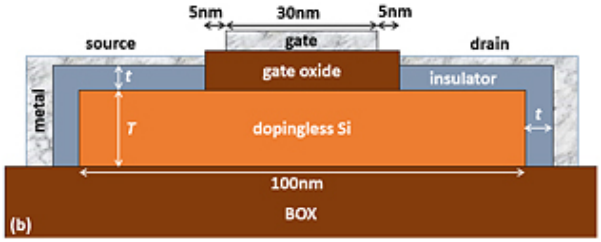

Fig. 1. The simulated dopingless Si FETs with MIS contacts. Following parameters are constant for both devices in all simulations: gate effective oxide thickness (*EOT*) of 1 nm, gate length of 30 nm and gate-SD offset of 5 nm. *T*: dopingless Si body thickness. *t*: insulator thickness. BOX: buried oxide.

Impacts of the insulator material parameters, such as *t*, *k* and E_g and χ_e, on the electrical characteristics of the proposed device are exhibited in Fig. 2(a-c), respectively. A thinner *t* promises higher I_{DS} by lowering the effective tunneling resistance at MIS contacts (Fig. 2(a)). A higher k value of the insulator at the MIS contact enhances the on-current (Fig. 2(b)), and which can be explained by the higher induced electron density in a wider area benefiting the carrier conduction. For a given WF_{SD}, on the other hand, if insulator E_g is decreased by rising its valence band edge, no difference on the electrical characteristics is observed (not shown). It is due to the fact that the electron tunneling probability is a function of barrier height ϕ between the metal WF_{SD} and insulator χ_e at the source MIS contact (between the semiconductor and insulator χ_e at the drain MIS contact). Therefore, Fig. 2(c) shows the transfer characteristics for different ϕ and t with a given WF_{SD}. The on-current increases with decreasing ϕ due to higher tunneling probability, and the enhancement is less obvious for a thinner t. In addition, the on-currents also exhibit strong dependence on ϕ by changing WF_{SD} (Fig. 2(d)) for the same reason.

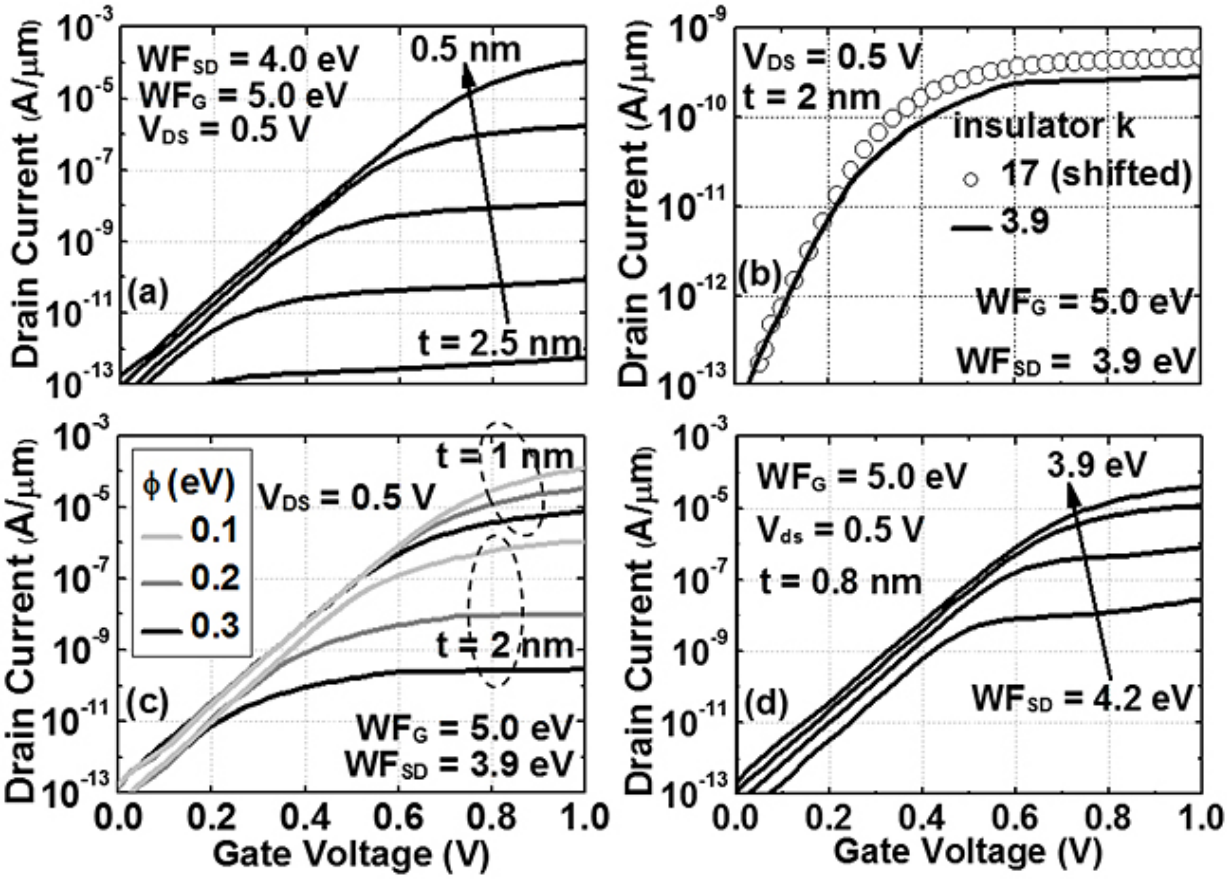

Fig. 2. Transfer characteristics of dopingless Si FETs (Fig. 1) with different (a) *t*, (b) *k*, (c) ϕ and (d) WF_{SD} at the MIS contacts. Besides those specified in the legends, the material parameters of the insulator (SiO_2) are specified by: ε = 3.9, E_g = 9 eV and χ_e = 0.9 eV. The curve with k = 17 in (b) has been shifted by +50 mV for a clear comparison.

Dopingless Si FETs with MS and MIS in parallel and with MIS only at SD contacts have been studied. It is found that if MS and MIS contacts are in parallel, currents may be mainly pathing through the MIS contacts for a given SD metal workfunction when the insulator thickness is thin enough. For the proposed device with MIS SD contacts only, the on-current can be improved by reducing the physical thickness, lowering the potential barrier height and increasing the dielectric constant of the insulator at the MIS contact. A lower effective WF_{SD} would boost the on-current by increasing electron tunneling probability at MIS contact as well, and which is achievable in reality by an insulator depinning the metal Fermi level for dopingless Si. In addition, it is also found that a thicker dopingless Si body increases the off-current owing to the loss of gate controllability in depth. This work combines the charge plasma concept in dopingless semiconductor and MIS ohimc contact, and predicts the electrical characteristics of the proposed device. It provides a general guideline with physical insights for designing dopingless FETs with high-k insulator at the SD MIS contacts.