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Ultra low-temperature microwave annealing for ultra-shallow junctions and P-MOS devices

Wen-Hsi Lee* ,Ming-Han Tsai, Chi-Ting Wu,Shao-Yu Hu
Electrical Engineering Department, National Cheng Kung University
leewen@mail.ncku.edu.tw

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Low energy ion implantation and low-temperature microwave annealing were used in this study to fabricate ultra-shallow junctions (USJs). A two-steps modulatory microwave annealing (MWA) process was employed to recover and activate a boron (400 eV) implanted silicon wafer. In the first step, 2.4 kWatt high power MWA was used to regrow an amorphous layer with the crystal silicon phase and thus enhance MWA absorption. After crystal silicon regrowth, 0.6 kWatt low power MWA was used to activate the implanted boron. The SIMS profile shows that the junction depth @5e18 was 13.5 nm, which is able to meet the requirement of the 20 nm VLSI process.

As gate length decreases, the extension junction depth must also be scaled down, and the sheet resistance must be reduced. Figure 1 shows the current trends in semiconductors with regard to these factors. One of the main difficulties in achieving smaller devices is the formation of annealed ultra-shallow junctions (USJs) in the S/D extension regions, especially with regard to transient-enhanced diffusion (TED) and electrical deactivation [1,2].

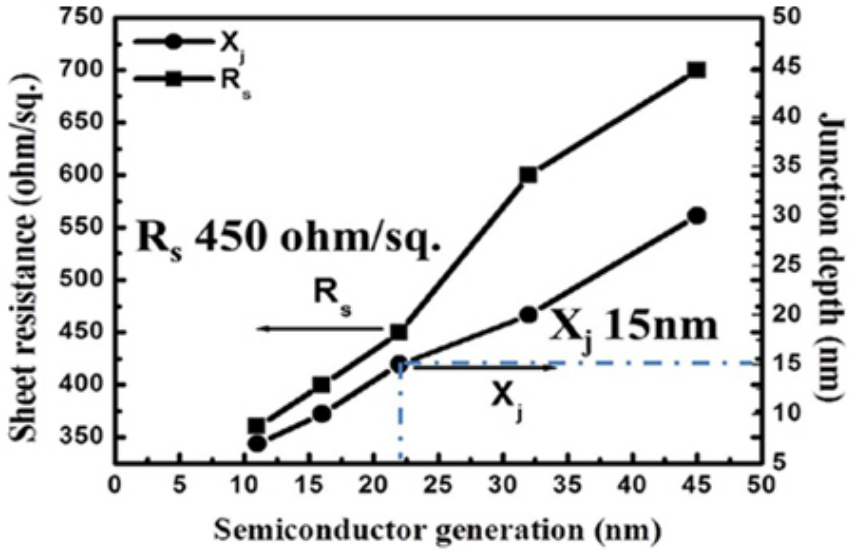

Figure 1 Current trends in semiconductors with regard to X_j and R_S

Solid-phase epitaxial regrowth (SPER) is required to repair the damage that occurs in the implantation process. Previous studies on the use of MWA to regrow an amorphous layer reported that the power and time requirements were related to the dopant type and dopant concentration used. In this case, 2400 W (~500°C) 5.8 GHz microwave power was employed. Figure 2 shows TEM cross-sectional images of the implanted silicon after annealing at 2400 W for 300 s.

Before annealing, the silicon layer was damaged due to the implantation energy and an amorphous silicon layer (a-layer) of 35.14 nm was formed. After MWA at 2400 W for 300 s, the a-layer regrew to crystalline silicon.

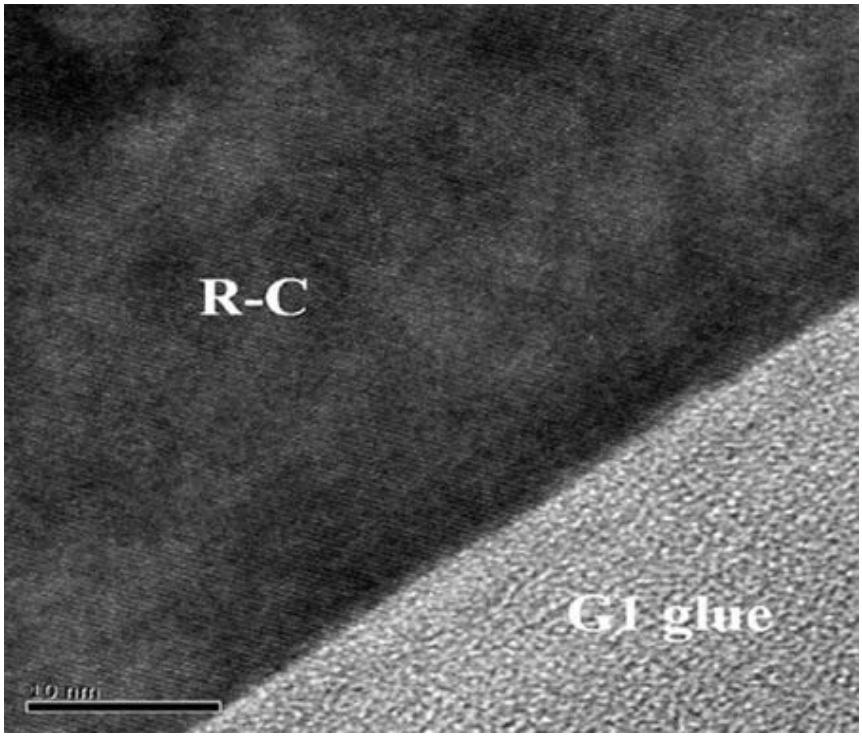

Figure 2 The thickness of the amorphous layer in a TEM cross section image after 2400 W MWA for 300 s

Raman spectroscopy was adopted to characterize the implanted sample after MWA. The spectra of the samples before and after 2400 W annealing are nearly identical. In contrast, the spectra of the samples after 600 W annealing show no recognizable peaks around 470 cm-1. This suggests that annealing with a higher power can regrow the crystalline silicon more effectively, as shown in Figure 3

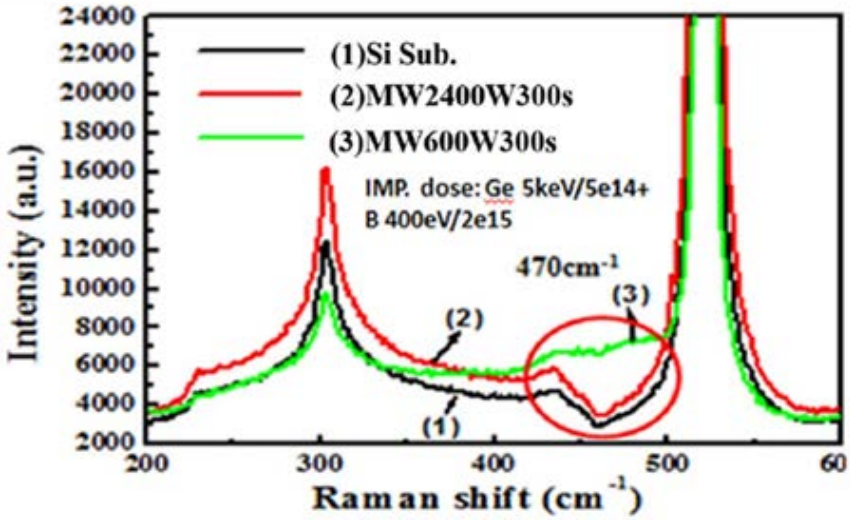

Figure 3 Raman profile of MWA2400W300s and 600W300s

Figure 4 shows the sheet resistance of the annealed samples. The sheet resistance of the sample after 2400 W annealing for 300 s is ~740 Ω/sq., which is still too high to meet the device's requirement with regard to the current process (~500 Ω/sq.). Higher resistance is directly related to a low level of activation, and the sheet resistance of the annealed samples increased along with the annealing time. This indicates that de-activation occurred, which commonly happens with conventional thermal annealing. The lowest value of resistance was 436 Ω/sq., which was achieved with 2400 W for 300 s in the first step and 600 W for 600 s in the second step. When the annealing time was 600 s, the resistance slowly increased again due to de-activation. Table 1 shows the result of the Hall measurements, which correspond to Figure 4. With the two-steps MWA process, the carrier concentration increases along with the annealing time, up until 600 s.

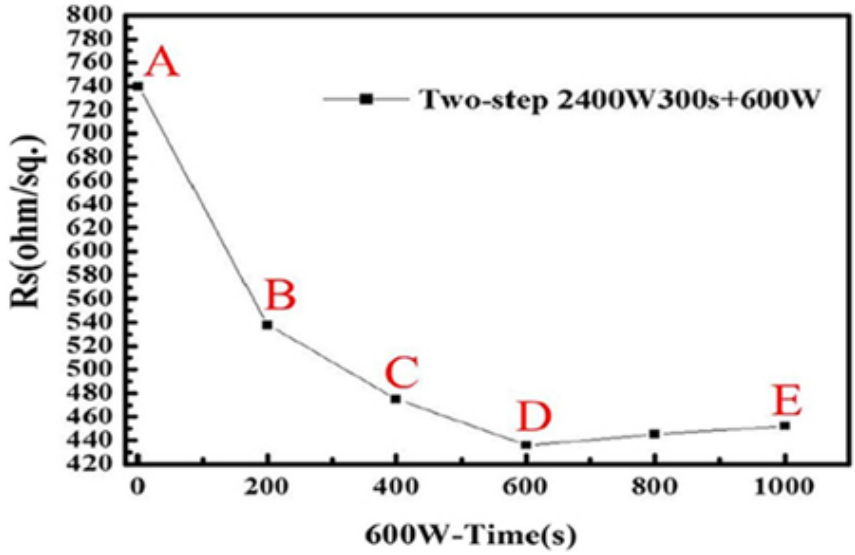

Figure 4 The sheet resistance of samples after two-steps annealing

Table 1 Results of Hall measurements for various annealing conditions

Remark	*Annealing*	*Resistivity*	*Mobility* (μ)	*Concentration* (n)
A	2400W300s	6.27E+02	3.87E+00	3.67E+15
B	2400W300s+600W200s	4.03E+02	4.28E+00	5.72E+15
C	2400W300s+600W400s	3.98E+02	4.19E+00	5.92E+15
D	2400W300s+600W600s	3.65E+02	4.13E+00	6.47E+15
E	2400W300s+600W1000s	4.72E+02	2.83E+00	5.54E+15

The results for the sheet resistance indicate that the two-steps MWA has excellent performance with regard to activation. With the single-step MWA it is difficult to attain both SPER and activation without de-activation. The two-step MWA thus provides an effective way to achieve both SPER and activation.

Figure 5 shows the SIMS profile of the implanted silicon after annealing. The junction depth defined at a background concentration @5e18 was 13.5 nm.

The diffusion control of the two-steps MWA process is able to meet the requirements of current devices, where the junction depth should be less than 15 nm. In this curve, one can see the diffusion depth of the microwave annealed samples is similar to the diffusion depth of the as-implanted samples, indicating that there is almost no boron diffusion after MWA.

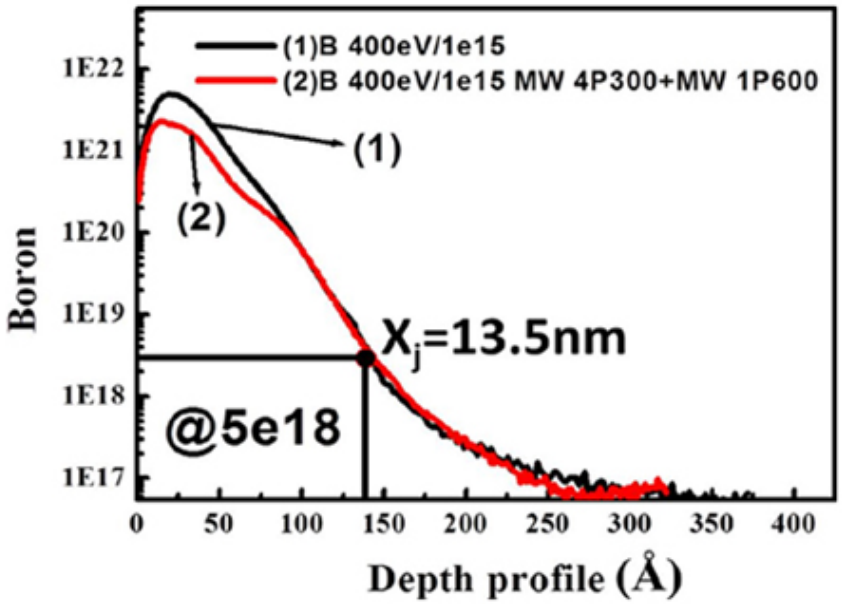

Figure 5 The SIMS profile of the implanted silicon before and after two-steps MWA

Figure 6 shows the transfer characteristic of the P-MOS device at Vds bias (–0.05 V). It can be seen that when the gate voltage changes the size of the inversion layer channel will also change, and so this measurement method can be used to observe the operation of the switching element and the switching current value of the voltage ratio. The current on/off ratio (Ion/Ioff) is higher than 2×10^6 (Vds = –0.05 V), which indicates that the two-steps modulatory MWA is able to achieve effective activation.

Table 2 shows the S.S., Ion/off ratio and Vth of the devices after MWA under different conditions. The device subjected to two-steps MWA (2400 W 300 s + 600 W 600 s) has the lowest

Vth. It also has the lowest S.S., which means it has the best ability to control the sub-threshold current. In these four devices, the largest Ion/off ratio is 2.203×10^6, and the smallest is 2.024×10^6. There are no significant differences among the Ion/off ratios of these four devices. However, it can be seen from the ID–VG results that the two-steps MWA process has much better control over the leakage current. The single-step MWA in the closed state leads to a more significant leakage current, and the occurrence of gate-induced drain leakage. In contrast, the two-steps MWA leads to a small off state leakage current, and the open circuit current in significantly greater. It can thus be seen that ion implantation has a good effect on the activation of the device, effectively reducing the leakage current and enhancing the open circuit current.

The results in Table 2 show that the devices annealed with two-steps microwave 4P300s + 1P600s (2400 W 300 s + 600 W 600 s) had the best characteristics. Furthermore, the results also show that the characteristics of the two-steps MWA devices are better than those of the one-step MWA devices.

Table 2 The sheet resistance, S.S., $I_{on/off}$ ratio and V_{th} of devices produced with MWA under different conditions

	Rs(ohm/sq.)	V_{th}(V)	SS (mV)	$I_{on/off}$
4P300s	740	–0.24	–97.6934	2.024×10^6
4P300s + 1P200s	538	–0.32	–96.723	2.139×10^6
4P300s + 1P400s	475	–0.38	–96.142	2.113×10^6
4P300s + 1P600s	436	–0.15	–92.5926	2.203×10^6

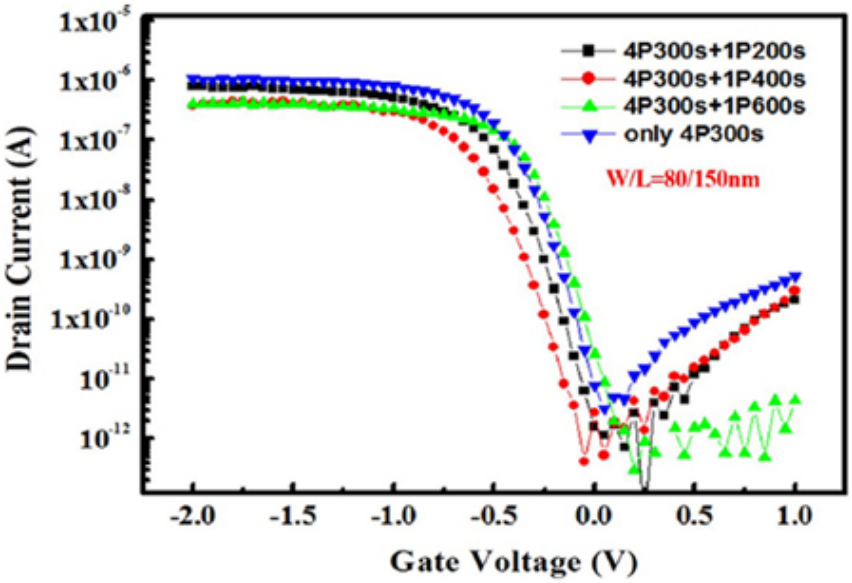

Figure 6 The IDVG curves of P-MOS devices produced with different MWA processes

Figure 7 shows the ID–VD curves of the devices produced with two-steps MWA (2400 W 300 s + 600 W 600 s). It can be seen that the device is functional when VG ranges between –0.5 V and –2 V. The I D–VD characteristic shows that the individual output current at different biases is large, higher than 1×10^{-5} A. Moreover, the two-steps MWA device have normal FET operations, with good linear and saturation regions. The fact that ID has good linearity with respect to VD suggests that the parasitic series resistance is low, and thus Schottky junctions are do not occur. It is thus clear that MWA can effectively activate doping after implantation.

Table 3 shows compares the conventional and MWA processes. Rapid thermal annealing (RTA) methods are used to reduce the diffusion of dopants during heating, the most common of which are lamp and laser annealing [3]. Spike and flash annealing also use high annealing temperatures and a short annealing time. The activation behavior with spike and flash annealing is rather large, and the ultra-short annealing time causes only limited diffusion. However, both approaches have some disadvantages. The ultra-high heating rate can cause thermal shocks and damage the structure of the material, while the ultra-short annealing time is not enough to re-crystalize the amorphous layer, and the remaining defects may cause junction leakage current [4] MWA is a promising method to form advanced USJs, and has the benefits of a low annealing temperature and long annealing time. Because the heat from microwaves is generated inside the material, MWA can effectively activate the dopant at low temperature, without dopant diffusion [5].

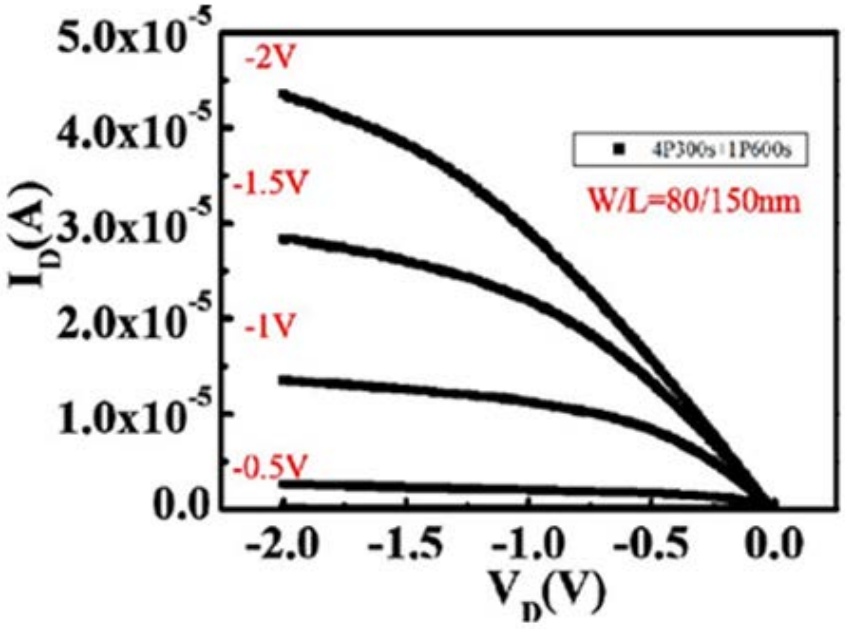

Figure 7 TheID–VDcurves of the P-MOS devices

Table 3 Comparison between conventional and microwave annealing for USJ

ultra-shallow junctions Technology	Implantation (ultra-shallow junctions)	Annealing	Advantages	Disadvantages
typical	Ge+C+B	Spike Flash Laser	High throughput	1.High temperature 2.High cost •with C implantation •Low yield (thermal shock) •High annealing machine cost
MWA	Ge+B	Microwave + Microwave	1.Low temperature 2.Low resistivity 3.Low cost •without C implant. •high yield(no thermal shock) •low annealing machine cost	Medium throughput

This work has demonstrated that two-steps MWA using two different powers is a viable means of dopant activation and re-crystallization in ion-implanted silicon.

References:

1. Agarwal, A., Gossmann, H. J., Eaglesham, D., Pelaz, L., Jacobson, D., Haynes, T., Erokhin, Y.E. (1997) 'Reduction of transient diffusion from 1–5 keV Si+ ion implantation due to surface annihilation of interstitials', Appl. Phys. Lett., Vol. 71, p.3141.
2. Pawlak, B., Vandervorst, W., Smith, A., Cowern, N.E.B., Colombeau, B. (2005) 'Enhanced boron activation in silicon by high ramp-up rate solid phase epitaxial regrowth', *Appl. Phys. Lett.*, Vol. 86, p.101913.
3. Pelaz, L., Jaraiz, M., Gilmer, G.H., Gossmann, H-J., Rafferty, C.S., Eaglesham, D.J. and Poate, J.M. (1997) 'B diffusion and clustering in ion implanted Si: the role of B cluster precursors', Appl. Phys. Lett., Vol. 70, p.2285
4. Hsueh, F.K., Lee, Y.J., Lin, K.L., Current, M.I., Wu, C.Y. and Chao, T.S. (2011) 'Amorphous-Layer Regrowth and Activation of P and As Implanted Si by Low-Temperature Microwave Annealing', IEEE Electron Device Lett., Vol. 58, p.2088.
5. Yamaguchi, T., Kawasaki, Y., Yamashita, T., Yamamoto, Y., Goto, Y., Tsuchimoto, J., Kudo, S., Maekawa, K., Fujisawa, M. and Asai, K. (2010) 'Low-resistive and homogenous NiPt-silicide formation using ultra-low temperature annealing with microwave system for 22nm-node CMOS and beyond', International ElectronDevices Meeting, San Francisco, USA, 6–8 December, pp.576–579.