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High Performance Poly Si Junctionless Transistors with Sub-5nm Conformally Doped Layers by Molecular Monolayer Doping and Microwave Incorporating CO_2 Laser Annealing for 3D Stacked ICs Applications

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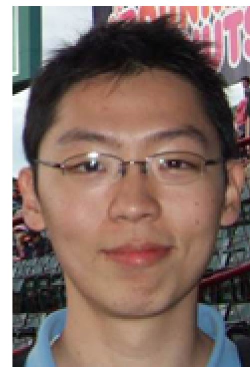

Reducing the physical size of metal-oxide-semiconductor field-effect transistors (MOSFETs) has been the mainstream in the semiconductor industry, enabling extraordinary improvements in the switching speed, device density, functionality and cost of microprocessors over the past few decades. Device scaling, however, inevitably leads to the short channel effects and increases the subthreshold leakage current and power dissipation. Apart from enhancing the gate control, reducing the junction depth is another approach to minimize the source-to-drain leakage current. Therefore, this publication is devoted to investigate the impact of an ultrashallow and shell doping profile (depth < 5 nm and abruptness ~ 0.6 nm/dec, formed by a damage-free and self-limiting chemical monolayer doping technique, activated by low temperature microwave annealing) on the electrical characteristics of nanoelectronic devices for low power applications.

Compared to a conventional MOSFET, a junctionless transistor possesses the simplicity of fabrication and the immunity of mobility degradation at the channel-oxide interface. Furthermore, a junctionless transistor with a multigate configuration showing the ideal subthreshold swing (SS) ~ 60 mV/dec has been demonstrated theoretically and experimentally. Hence, junctionless transistors are the focused devices in the publication.

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