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Voltage-Aware Chip-Level Design for Reliability-Driven Pin-Constrained EWOD Chips

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Digital microfluidic biochips (DMFBs) have emerged as useful biotechnology applications because of high throughput, high sensitivity, and low cost compared to conventional laboratory procedures. Because they can precisely control the movements of nanoliter droplets containing samples and reagents, DMFBs have used to realize various applications such as DNA sequencing, immunoassays, environmental monitoring, and clinical diagnosis. The most promising technology is an electrowetting-on-dielectric (EWOD) chip. As Figure 1.(a) shows, a general EWOD chip consists of a two-dimensional (2D) electrode array, peripheral devices (e.g., optical detector and dispensing port), and surrounding electrical pads. The sample carriers (i.e., droplets) on the array are controlled by underlying electrodes. By using time-varying voltage to actuate the electrodes, droplets can be moved toward the actuated electrode due to the electrowetting phenomenon. Many basic fluidic operations, such as mixing, transporting, and splitting can be carried out by manipulating the droplets. As the complexity of biochemical assay increases, comes the corresponding high complexity of EWOD chips. Undoubtedly, powerful computer-aided-design (CAD) tools are demanded to design the EWOD chip. With CAD tools, EWOD chips can be designed with automation, reducing the human effort and enable high productivity of EWOD chips.

As the chip size increases, the number of control pins must be limited because these pins are controlled by an external controller with a limited number of signal ports. This triggers the demands of pin-constrained DMFBs (PDMFBs). To solve this problem, broadcast addressing technique utilizes the concept of pin sharing to assign a single control pin to multiple electrodes without affecting the assay execution. However, because pin sharing may cause excessive applied voltage, it also results in trapped charge problem which is a phenomenon that the charge becomes trapped in the dielectric insulating layer of the chip, effectively reducing the electrowetting force. That is, it will reduce the reliability of EWOD chips. Except for the trapped charge problem, the wire routing required to accomplish electrical connections also increases the design complexity of pin-constrained EWOD chips. This paper presents a well-designed CAD tool that can reduce pin count simultaneously keeping reliability of EWOD chips. The solution also provides a comprehensive routing solution for EWOD chip-level designs. The algorithm contains incremental search restraining the voltage and network-flow based pin-electrode progressive matching and rerouting technique to obtain feasible solution. The experimental results on a set of real-life applications demonstrated that the proposed approach was very effective and efficient.

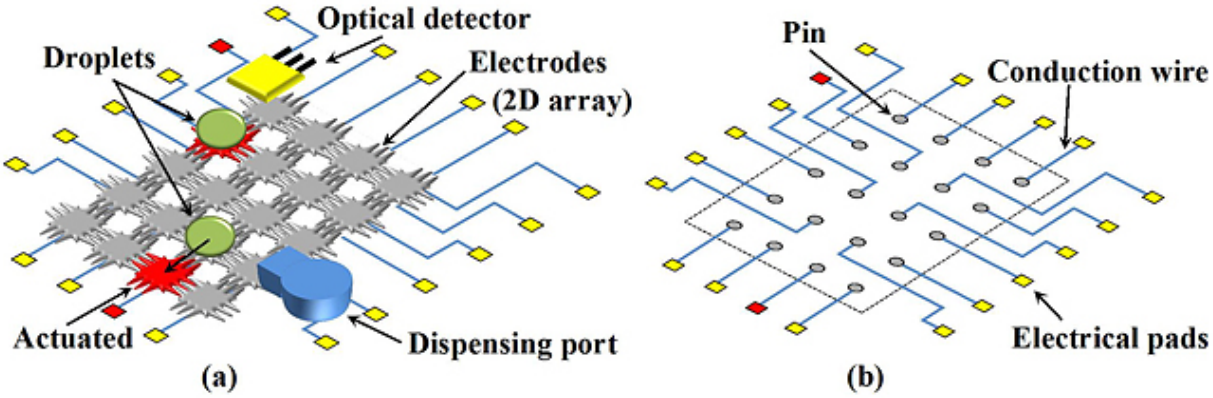

Figure 1. (a) The schematic view for EWOD chips. (b) Underlying electrical connections.

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