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Improved Poly Gate Engineering for 65 nm Low Power CMOS Technology

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As complementary metal oxide semiconductor (CMOS) technology aggressively scales down to improve the performance of CMOS devices, the poly gate formation process has been investigated intensively. However, the impact of poly grain structure on device characteristics has not received much attention. In this study, we investigate the impact of a novel poly deposition method on CMOS device characteristics including device mismatch (proportioned to $1/\sqrt{(W \times L)}$), I_{off}-I_{dsat}, short channel effect (SCE), and gate dielectric reliability. Experimental results reveal that the novel poly deposition method can improve device characteristics.

Devices used in this study were fabricated on p-type Si-<100> substrates using a standard low power 65 nm CMOS technology. An effective oxide thickness of roughly 1.9 nm ultra-thin gate dielectric was grown by pulsed radio-frequency decoupled plasma nitridation. Two different poly depositions with roughly 100 nm thickness are named Poly A and B, where Poly B is the novel deposition process. We used 3200 sccm Si_2H_6/H_2 gas for Poly B instead of 60 sccm SiH_4 gas for Poly A at the ambient temperature 710℃ and pressure 50 torr by low pressure chemical vapor deposition. Then, the poly patterning was performed using 193 nm dry lithography and accurate process controlled etching to control a 55 nm poly length. After poly patterning, the following processes were performed to form a MOSFET: 850℃ re-oxidation, spacer, pocket/lightly doped drain (LDD), and source/drain implants with subsequent rapid temperature anneal. Finally, the interlayer dielectric of the contact, intermetal dielectrics of the metal, and via layers were processed for back end of the line for MOSFETs.

To examine the impact of the novel poly deposition process on device characteristics, the device I_{dsat} asymmetry is examined. In this study, I_{dsat} asymmetry is defined as 3 sigma (σ) of ΔI_{dsat} ($I_{dsat\_forward}$ (drain to source) – $I_{dsat\_reverse}$ (source to drain)). Fig. 1 shows I_{dsat} asymmetry for devices with various poly width (W) and length (L). Since a smaller slope in I_{dsat} asymmetry vs. $1/\sqrt{(W \times L)}$ plot has better device symmetry, results in Fig. 1 reveal that Poly B has better I_{dsat} symmetry than Poly A for both N and PMOSFETs. Besides, we use poly width = 1 μm and length = 70, 60, and 55 nm MOSFETs to examine I_{off}-I_{dsat} plot to see the impact of the novel poly process on device performance. As shown in Fig. 2, I_{off}-I_{dsat} of Poly B has 5% ~ 8% I_{dsat} gain at a similar I_{off} for both N- and PMOSFETs. In other words, Poly B can improve the I_{off} current.

In addition to I_{dsat} symmetry and I_{off}-I_{dsat} characteristics, we also examine drain-induced barrier lowering (DIBL) to evaluate SCE of MOSFETs. DIBL is defined as (V_{tlin} - V_{tsat}), where V_{tlin} and V_{tsat} are linear region and saturation region threshold voltage, respectively. As seen in Fig. 3, Poly B has lower DIBL through various poly lengths for both N- and PMOSFETs. Thus, Poly B can improve SCE. Two reasons are responsible for the improved SCE. One is that Poly B produces a small poly grain to suppress source/drain and LDD implant species diffusion through poly into channel of MOSFETs. The other is that Poly B provides a straight poly profile after etching. Because the poly grain may affect the poly profile and also affect gate dielectric quality,

the voltage ramp dielectric breakdown (VRDB) method is measured for gate oxide integrity verification. The breakdown voltage for poly A and B processes are measured on finger shape test vehicle (which can diagnose gate oxide quality at bottom edge of the poly) as shown in the inserted diagram of Fig. 4(a). As seen in Fig. 4, Poly B improves the VRDB and uniformity. Thus, Poly B can also improve gate dielectric quality

In conclusion, the device asymmetry estimated by I_{dsat} is improved by using the novel poly deposition because a better poly profile after poly patterning is produced. I_{off}-I_{dsat} relationship reveals that the improved poly deposition can decrease leakage current and also improve the short channel effect. The gate dielectric quality is also examined by VRDB and results show that the novel poly deposition produces a better gate dielectric breakdown immunity and uniformity.

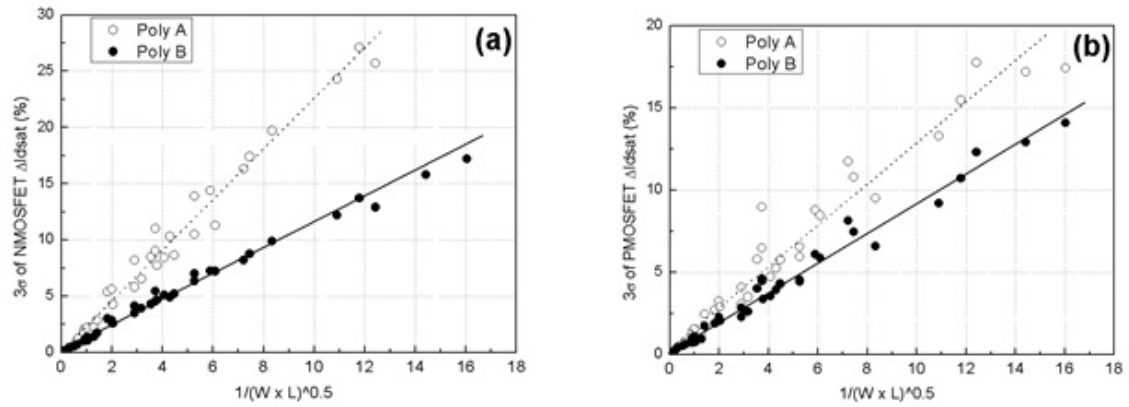

Fig. 1. Relationship of I_{dsat} asymmetry and $1/\sqrt{(W \times L)}$ with different poly deposition processes for (a) NMOSFET and (b) PMOSFET.

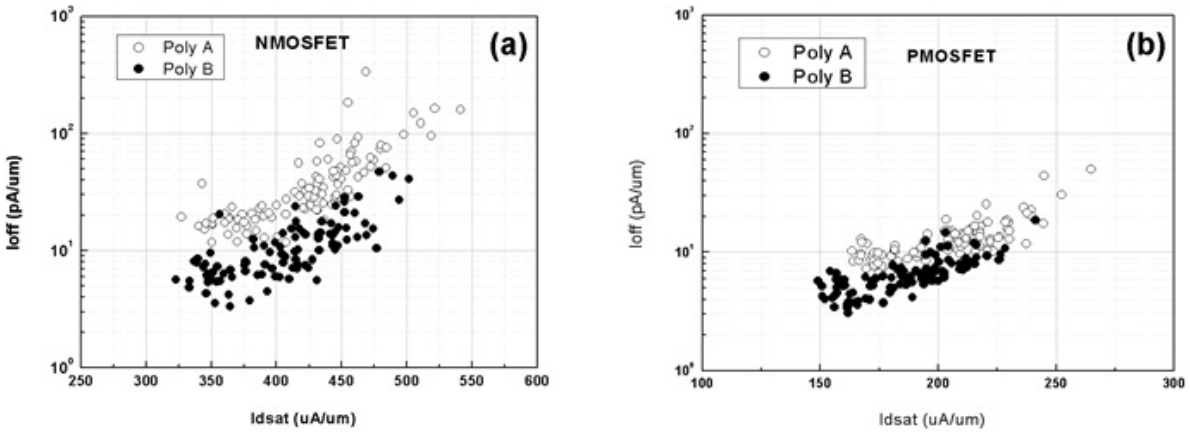

Fig. 2. Relationship of I_{off} and I_{dsat} with different poly deposition processes for (a) NMOSFET and (b) PMOSFET.

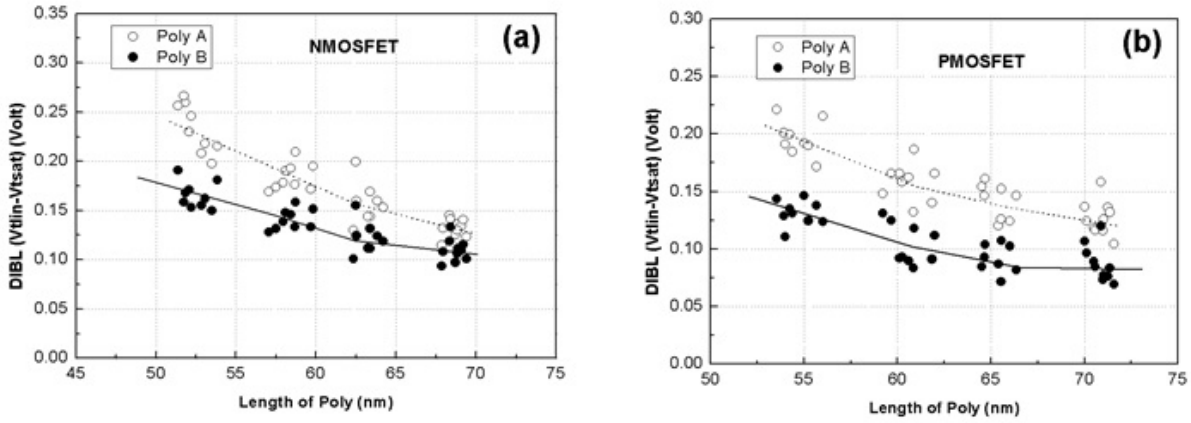

Fig. 3. Relationship of drain-induced barrier lowing (DIBL) and poly length with different poly deposition processes for (a) NMOSFET and (b) PMOSFET.

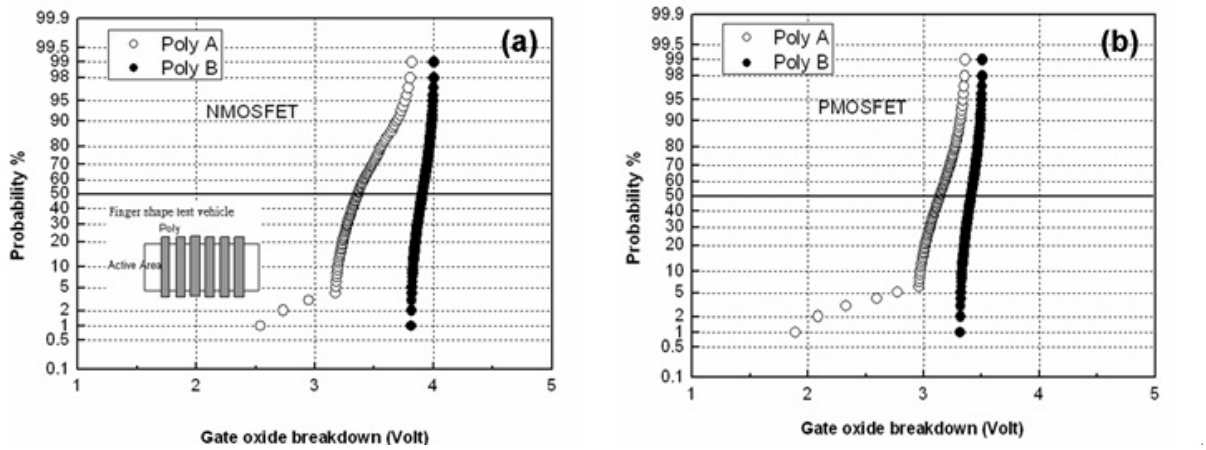

Fig. 4. Voltage ramp dielectric breakdown (VRDB) probability plot of different poly deposition processes for (a) NMOSFET and (b) PMOSFET.