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Temperature-Dependent Characteristics of a Pseudomorphic High Electron Mobility Transistor (PHEMT) with Graded Triple Delta-Doped Sheets

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Recently, the prosperous designs of various compound semiconductor devices, such as the pseudomorphic high electron mobility transistors (PHEMTs), heterostructure field-effect transistors (HFETs), and heterojunction bipolar transistors (HBTs) have been widely applied in monolithic microwave integrated circuits (MMICs). Also, doped-channel field-effect transistors (DCFETs), due to the specific doped-channel structures, have demonstrated excellent linearity characteristics. However, the intrinsic ionized impurity scattering in DCFETs seriously degrades carrier transport properties. Experimentally, for the materials used in Schottky and buffer layers, the InGaP layer is a good candidate. It provides several advantages such as (1) the absence of Al which could eliminate the problem associated with DX centers, (2) the relatively low surface recombination velocity and results in low 1/f noise figure, (3) the high etching selectivity between InGaP and GaAs causes the easy control in gate recess, and (4) InGaP is relatively difficult to be oxidized which makes a high-yield process.

In this work, an interesting InGaP/InGaAs/GaAs double channel PHEMT with graded triple delta-doped carrier supplier layers is fabricated and demonstrated. The double channel design is used to effectively increase the total thickness of channel and still maintain the In mole fraction as high as 0.2. Moreover, the use of graded triple delta-doped carrier supplier layers ($\delta(n^+)$ = 3, 2 and 1×10^{12} cm^{-2}) could lead to the uniform distribution of carriers in the double channel layers. In addition, high conductance-band discontinuity ($\triangle E_C$) up to 0.38 eV at $In_{0.49}Ga_{0.51}P$ barrier/ $In_{0.2}Ga_{0.8}As$ channel heterostructure is obtained to improve the channel confinement capability. Therefore, the low leakage current, high breakdown voltage, high transconductance, high drain current drivability, good channel confinement, and good microwave performance are simultaneously expected. The device characteristics over wide temperature range (300～450 K) are systematically investigated. Furthermore, the simulated current-voltage (*I-V*) characteristics at 300K show excellent agreement with experimental results.

The corresponding conduction-band diagram of the studied device is illustrated in Fig. 1. The layer structure consisted of a 0.5- μ m GaAs buffer layer, a 450-Å $In_{0.49}Ga_{0.51}P$ buffer layer, a delta-doped sheet $\delta_3(n^+) = 1 \times 10^{12}$ cm^{-2}, a 50-Å $In_{0.49}Ga_{0.51}P$ spacer layer, a 100-Å $In_{0.2}Ga_{0.8}As$ channel layer, a 40-Å GaAs spacer layer, a delta-doped sheet $\delta_2(n^+) = 2 \times 10^{12}$ cm^{-2}, a 40-Å GaAs spacer layer, a 100-Å $In_{0.2}Ga_{0.8}As$ channel layer, a 50-Å $In_{0.49}Ga_{0.51}P$ spacer layer, a delta-doped sheet $\delta_1(n^+) = 3 \times 10^{12}$ cm^{-2}, a 160-Å $In_{0.49}Ga_{0.51}P$ Schottky barrier layer, and a 300-Å GaAs ($n^+ = 4 \times$

10^{18} cm^{-3}) cap layer. After epitaxial growth, the device was processed by standard photolithography, conventional vacuum evaporation, and lift-off techniques. First, the mesa isolation was performed by wet chemical etching. Drain and source Ohmic contacts were formed on n^+-GaAs cap layer by alloying evaporated AuGe/Ni/Au metals at 350℃ for 30s. Subsequently, the n^+-GaAs cap layer was removed by wet etching. The dielectric (SOG) thickness is 1 μm. The gate windows with 1 μm were defined and re-flowed the photoresist by baking the sample at 140℃ for 1 minute. The sub-micron gate window with practical gate length of L_g = 0.8 μm was obtained. Finally, the gate Schottky contact was achieved by evaporating Au metal on the undoped $In_{0.49}Ga_{0.51}P$ Schottky barrier layer.

Figure 2 shows the typical common source *I-V* characteristics of the studied practical device at different temperatures. At room temperature, the experimental (solid lines) and simulated (dashed lines) results are shown in the inset of Fig. 2. The applied gate-source voltage is kept at V_{GS} = -1 V/step. Obviously, the simulated data generally agree with experimentally measured results. As shown in the inset, the available drain saturation current I_{DS}, measured at V_{GS} = 1.5 V, is as high as 396 and 408 mA/mm at room temperature for experimental and simulated devices, respectively. In addition, the studied practical device shows good pinch-off and saturation characteristics at different temperatures due to good carrier confinement and reduction of gate leakage current.

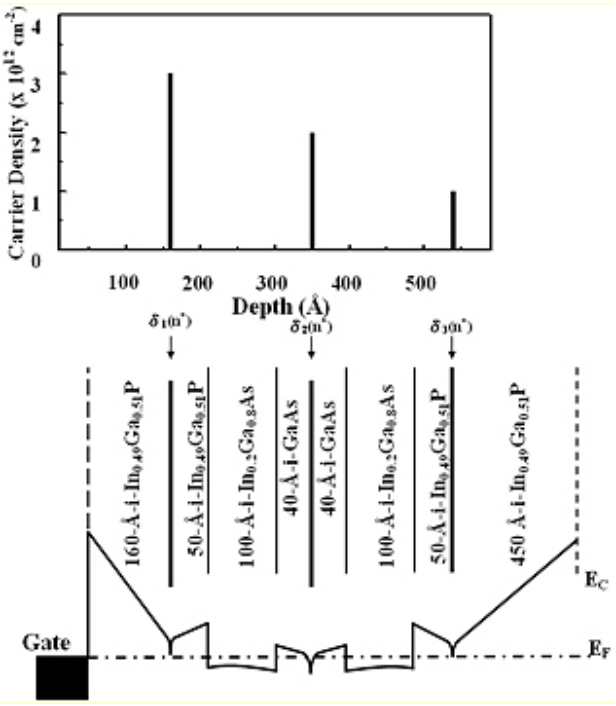

Fig. 1 The corresponding conduction-band diagram of the studied device.

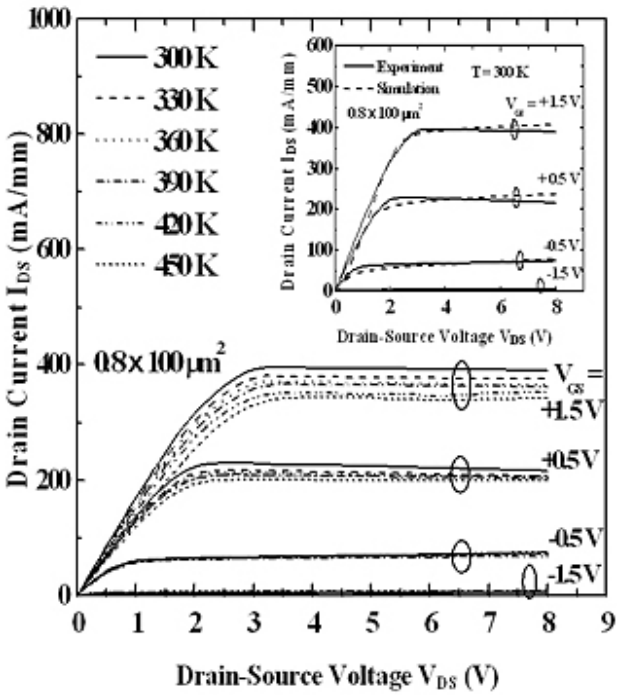

Fig. 2 The typical common-source output current-voltage characteristics of the studied practical device at different temperatures. The inset shows experimental (solid lines) and simulated (dashed lines) results of typical common-source output current-voltage characteristics of the studied devices.

The I_{DS} and extrinsic transconductance g_m as a function of V_{GS} at different temperatures are illustrated in Fig. 3. The related experimental (solid lines) and simulated (dashed lines) results at room temperature are shown in the inset of Fig. 3. The biased voltage is fixed at drain-source voltage of V_{DS} = 3.5 V. The maximum values of transconductance $g_{m,max}$ are 176 and 175 mS/mm for simulated and experimental devices, respectively. Due to the good carrier confinement and the employed graded triple δ-doped sheets, the studied device shows good linearity in g_m behaviors.

Meanwhile, these good behaviors demonstrate that most of electrons are confined at the double InGaAs channel. Due to the increase of background carrier concentration and the reduction of electron mobility with increasing the temperature, the $g_{m,max}$ and I_{DS} are decreased. The operating voltage swings, defined as the V_{GS} regimes with the drop of 10 % from $g_{m,max}$, are 1.6 and 1.33 V at 300 and 450 K, respectively. This implies that the studied practical device has high V_{GS} swing even in the high-temperature region. Based on the low degradations of $g_{m,max}$ and V_{GS} operation regime with increasing the temperature, the studied device is relatively temperature independent and suitable for high power and low distortion circuit applications. In addition, the threshold voltage V_{th} values are -1.25 and -1.67 V for simulated and measured devices, respectively. The slight differences of subthreshold characteristics between measured and simulated results may be attributed to the leakage current path in the practical device and/or unexpected process conditions.

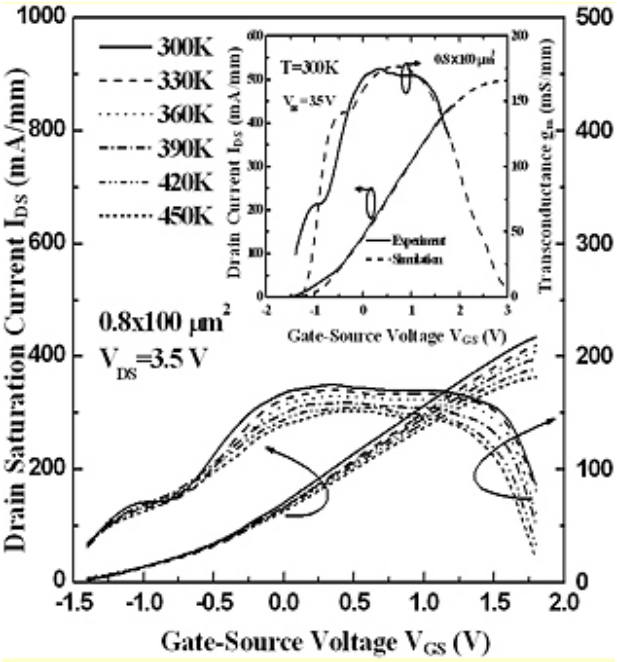

Fig. 3 Drain saturation current I_{DS} and extrinsic transconductance g_m versus gate-source voltage V_{GS} of the studied practical device at different temperatures. The inset shows experimental (solid lines) and simulated (dashed lines) results of drain saturation current I_{DS} and extrinsic transconductance g_m versus gate-source voltage V_{GS}.

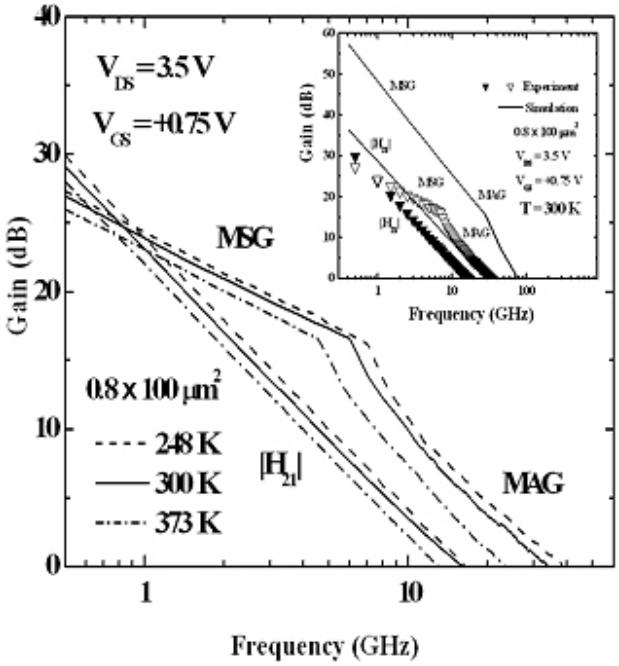

Fig. 4 The microwave performance of the studied practical device at 248, 300, and 373 K. The inset shows experimental and simulated microwave performance of studied devices. Symbols represent experimental results and solid lines denote simulated data.

The microwave characteristics of the studied practical device at 248, 300, and 373 K are illustrated in Fig. 4. The inset shows experimental and simulated microwave performance of the studied device at room temperature. The biased conditions are fixed at V_{DS} = 3.5 V and V_{GS} = 0.75 V. Symbols represent experimental results and solid lines denote simulated data. The maximum unit current gain cut-off frequency f_T and maximum oscillation frequency f_{max} are 16 (34.6) and 33.2 (97.5) GHz for experiment (simulated) device. The difference of microwave performance between experiment and simulated results may be attributed to the parasitic electrode capacitance, parasitic resistances, e.g., contact resistance of drain and source Ohmic contact and gate resistance, and parasitic inductance. The f_T value of the practical device is decreased from 17.3 to 13.9 GHz as the temperature is increased from 248 to 373K. The corresponding f_{max} is decreased from 35.1 to 30.4 GHz. Obviously, the f_T and f_{max} shows slight degradations with

temperature.

In conclusion, an interesting InGaP/InGaAs/GaAs double channel PHEMT with graded triple delta-doped sheets has been successfully fabricated and demonstrated. A theoretical analysis based on a 2-D semiconductor simulation package is used to study the device properties and compare the experimental results. Good agreement between the theoretical analyses and experimental results are found. In addition, the temperature-dependent characteristics of the practical PHEMT device are studied and demonstrated. From the experimental results, the improvements of device performance including the drain saturation current, transocnductance, and superior microwave performance are obtained. Therefore, the studied device provides the promise for high temperature and high performance microwave applications.