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On-Resistance Degradation Induced by Hot-Carrier Injection in LDMOS Transistors with STI in the Drift Region

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High-voltage devices are integrated into CMOS technologies to fulfill the trend of lower cost and smaller chip size in recent specific high-voltage products. Lateral DMOS (LDMOS) transistors are the suitable devices to be integrated into smart-power applications because of their compatibility with CMOS process. Because LDMOS devices are usually operated under high drain voltage (V_{ds}) and high gate voltage (V_{gs}), hot-carrier-induced degradation is a major reliability concern in LDMOS transistors. In this work, the phenomenon and mechanisms of hot-carrier-induced on-resistance (R_{on}) degradation in n-type LDMOS transistors with shallow trench isolation (STI) in drift region are investigated. Based on experimental data and technology computer-aided-design (TCAD) simulation results, the mechanisms responsible for R_{on} shift are discussed.

Fig. 1 shows the schematic cross section of the n-type LDMOS transistor used in this work. This device is integrated into a 0.25-μm CMOS process and features a STI in n^- drift region near the drain. The channel length is about 0.3 μm. The gate oxide thickness and gate width of the device are 30 nm and 10 μm, respectively. The operational voltages are V_{ds} = 40 V and V_{gs} = 12 V. To investigate hot-carrier-induced degradation, stressing under V_{ds} = 40 V and various V_{gs} is performed at room temperature with source and substrate connected to the ground. The stress tests are interrupted periodically to measure the degradation of device parameters including R_{on}. R_{on} (= V_{ds}/I_d, where I_d is drain current) is measured under V_{ds} = 0.1 V and V_{gs} = 12 V. Two-dimensional TCAD simulations are also performed to explain the experimental results.

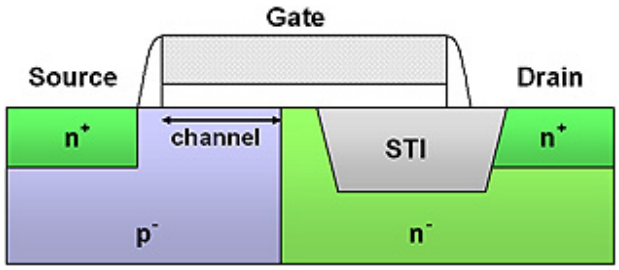
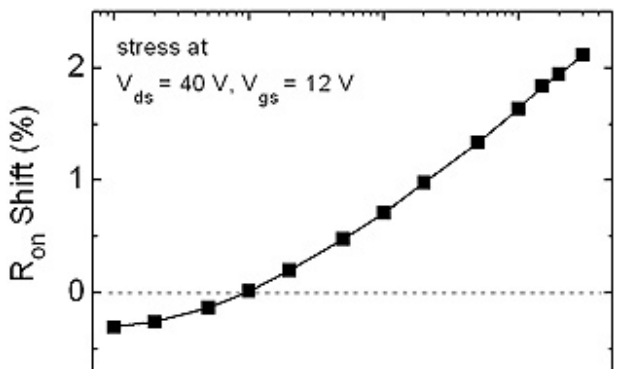


Fig. 1. Schematic cross section of the n-type LDMOS device used in this work.



Two substrate current (I_{sub}) peaks are observed in I_{sub}-V_{gs} characteristics in our LDMOS devices. The first I_{sub} peak occurs at V_{gs} = 4 V that is similar to the behavior in conventional MOSFETs. As V_{gs} > 8 V, I_{sub} rises again because of Kirk effect and the second I_{sub} peak occurs at V_{gs} = 12 V. When our LDMOS devices are stressed under

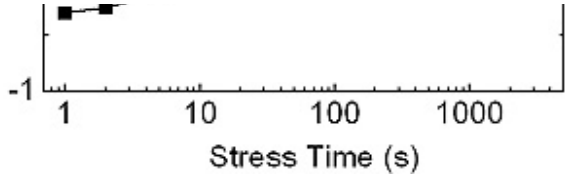


Fig. 2. R_{on} shift as a function of stress time for the device stressed under V_{ds} = 40 V and V_{gs} = 12 V.

V_{ds} = 40 V with various V_{gs} (2.5, 4, 8, and 12 V), the device stressed under V_{gs} = 12 V degrades the most. As a result, the following analysis is focused on the device stressed under V_{gs} = 12 V. Fig. 2 shows R_{on} shift as a function of stress time for the device stressed under V_{ds} = 40 V and V_{gs} = 12 V. An unexpected reduction in R_{on} is observed at the beginning of stress. When the stress time is shorter than 10 s, R_{on} is smaller than its fresh value (I_d increases). As the stress time is longer than 10 s, R_{on} is greater than its fresh value (I_d decreases).

To investigate the mechanism of R_{on} degradation, TCAD simulation results are analyzed. Fig. 3(a) shows simulated impact ionization (ii) rate along Si/SiO_2 interface when the device is biased at V_{ds} = 40 V and V_{gs} = 12 V. Results show that an ii peak exists at the STI corner closest to the channel. Another severe ii generation caused by Kirk effect occurs at the STI edge closest to the drain. Fig. 3(b) shows simulated vertical electric field (E_y) along the Si/SiO_2 interface under the same bias condition. Positive E_y indicates that the direction of E_y is pointing downward and is favorable for electron injection. Negative E_y, on the contrary, is favorable for hole injection. From Fig. 3(a) and Fig. 3 (b), the mechanisms of R_{on} degradation are suggested as follows. At the STI corner closest to the channel, energetic electron-hole pairs are generated because of severe ii generation. Holes are injected into STI because of negative E_y. Such a hot-hole injection may create hole trapping. Trapping of holes in STI induces negative mirror charges at Si/SiO_2 interface in drift region, resulting in an effective increase in drift region concentration. As a result, I_d increases and R_{on} decreases. This inference explains why R_{on} is reduced at the beginning of stress. On the other hand, the severe ii generation at the STI edge closest to the drain results in hot-electron injection because of positive E_y. Such an electron injection may create electron trapping and interface trap (N_{it}), leading to R_{on} increase. The damage created at the STI edge closest to the drain is expected to dominate R_{on} degradation as the stress time is longer. This explains why R_{on} is greater than its fresh value after 10 s as in Fig. 2.

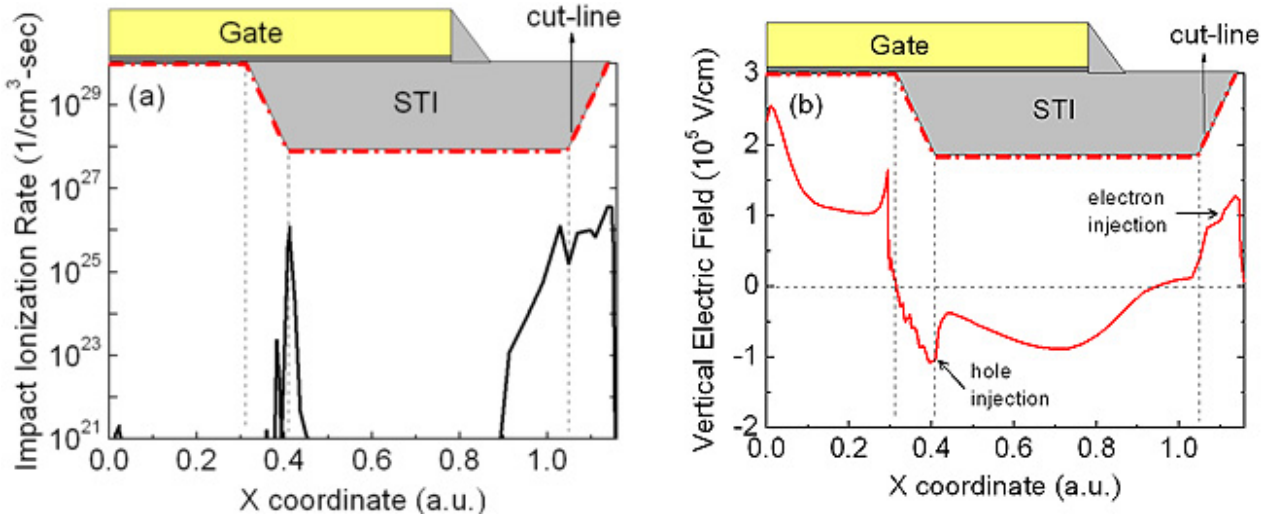


Fig. 3. Simulated (a) ii rate, (b) vertical electric field along the Si/SiO_2 interface under V_{ds} = 40 V and V_{gs} = 12 V.

To verify the existence of hole trapping, Fig. 4 shows I_d shift measured at different V_{gs} as a function of stress time for

the device in Fig. 2. When I_d is measured at low V_{gs} (= 3.5 V), the current path under STI is deeper. This argument can be confirmed in Fig. 5, where the simulated accumulated current as a function of the depth from Si/SiO_2 interface at the location of the STI corner closest to the channel is shown. The current is accumulated from the bottom of n^- region to Si/SiO_2 interface. Results show that the accumulated current near Si/SiO_2 interface under V_{gs} = 3.5 V rises less rapidly than that under V_{gs} = 12 V, indicating that current path is away from Si/SiO_2 interface at low V_{gs}. As current flows deeper, the effect of negative mirror charges on I_d increase is less apparent. Thus, I_d decreases monotonously during stress when I_d is measured at V_{gs} = 3.5 V as in Fig. 4. The results in Fig. 4 reveal that hole trapping is responsible for the unexpected R_{on} reduction in the early stage of stress.

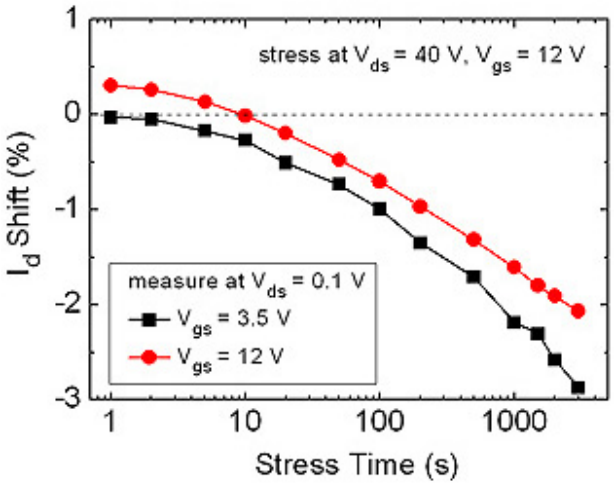


Fig. 4. I_d shift measured at different V_{gs} as a function of stress time for the device in Fig. 2.

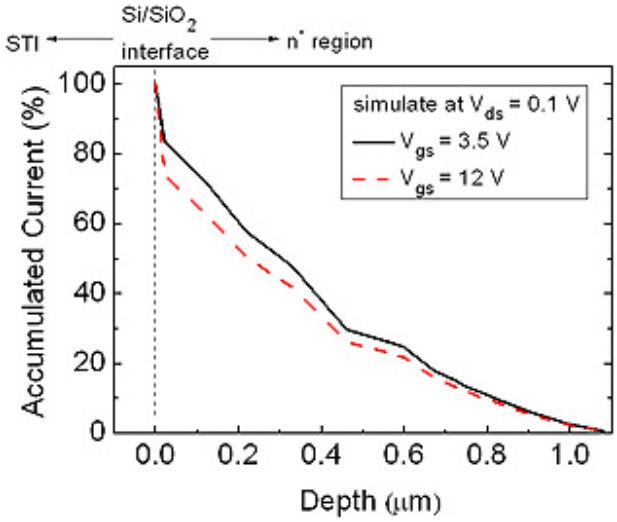


Fig. 5. Simulated accumulated current as a function of the depth from Si/SiO_2 interface at the location of bottom-left corner of STI.

In conclusion, the phenomenon and mechanisms of hot-carrier-induced R_{on} degradation in n-type LDMOS transistors with STI in drift region are discussed. R_{on} decreases at the beginning of stress but R_{on} increases afterwards. Experimental data and TCAD simulation results suggest that R_{on} reduction is attributed to hot-hole injection and trapping at the STI corner closest to the channel. According to results presented in this study, the unexpected R_{on} decrease should be paid special attention in evaluating LDMOS transistors' reliability.