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Degeneration of CMOS Power Cells After Hot-Carrier and Load Mismatch Stresses

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Abstract

In this letter, we investigate the performance degradation of nMOS transistors due to hot-carrier effect and load impedance mismatch. The DC and RF characteristics, such as drain current, threshold voltage, transconductance, output power, and power-added efficiency etc., are affected under hot-carrier effect. With load impedance mismatch, the transistors experience the reflected power from load and increase the energy of hot carriers. This effect will make DC and power performances degenerate heavily. In this paper, device characteristics were measured at 5.2 GHz.

I. INTRODUCTION

In sub-micrometer CMOS transistors, the channel length is scaled down and the electric field between drain and source becomes higher. The high lateral electric field in the MOSFETs induces hot carriers near the drain side which make the gate dielectric damaged and cause degradation of device characteristics. The hot carrier effects induce several degradations such as the shift of the threshold voltage, the degradation of drain current and decreasing transconductance (g_m)[1]. The cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) will also be affected, which induce the degradation of RF power performance at high frequency[2]. The increased random thermal motion of carriers in the channel after hot-carrier stress also increases the channel thermal noise and flicker ($1/f$) noise[3,4]. By considering the degradation in DC and RF performance of active devices, the reliability of circuits in RF communication system can be predicted.

The load-pull system is used to find the maximum output power of an active device when designing a power amplifier. The source and load impedances were tuned during the so-called “power contour” procedure. Usually, the load impedance for the maximum output power may not be the same as that of the conjugate matching for the optimal output return loss, hence the load reflection coefficient will not be zero. This mismatch will induce the reflected power from load at the drain terminal and produce heavier damage due to the hot-carrier effects. Therefore, if the quality of the matching network is not good enough, the reflected power will worsen the reliability of the circuits. Although load impedance mismatch is common in power amplifiers, the analysis of performance degeneration of transistor cells is not presented clearly yet.

Previous works about the reliability of MOSFETs only focused on the DC stress, or a dynamic stress at lower frequency[5,6]. However, these do not reflect the real operation situation of devices which are used in high-frequency and high-power circuits for wireless communication systems. It has been demonstrated that the degree of the degeneration depends on the quantity of load mismatch and the layout patterns[7]. It can be expected that the degradation will be more serious at high frequency and high power application.

This paper is focused on the degradation of power cells used for power amplifiers with high output power. In this work, the size and bias condition of the cells were designed for output power larger than 10dBm. The operation frequency is chosen to be 5.2 GHz that conforms to the application of IEEE 802.11a. Based on the measurement results, the hot-carrier effects resulted from reflected RF power from load impedance mismatch is much larger than that of DC stress at high bias voltages. The measurement results also show the relationship between the degradation of performances and the intensity of hot carrier effect resulting from DC or RF stresses.

II. EXPERIMENTS

In this work, the nMOS transistors were fabricated by using a 0.18 μm triple-well 1P6M CMOS technology. The size and bias of the cell was chosen to implement output power larger than 10 dBm. The drain current of the fresh cell is 24.54 mA with V_{gs} of 1.2 V and V_{ds} of 1.8 V. Figure 1 shows the layout diagram of the studied power cell. The cell is one sixteen-finger transistor module with channel width of 5 μm for each finger. The total channel width of the cell is 80 μm. The channel length is 0.18 μm. The size of the studied cell is 28.7 × 20.6 μm^2. The pads were added for on-wafer measurement.

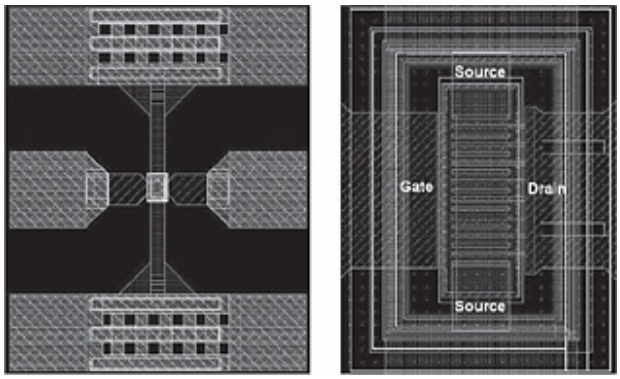


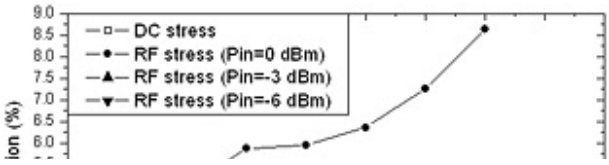
Fig. 1. (a) Layout pattern of the studied power cell. (b) Detail of the cell

In order to compare the effects of DC and RF stresses, two experiments were done. As other reliability tests, for the DC stress, the power cell was biased at high voltage with V_{gs} of 1.8 V and V_{ds} of 2.5 V. At this bias situation, the drain current was almost twice compared to normal operation of this cell. For the RF stress, the input power was set to be 0, -3, and -6 dBm under the bias conditions of V_{gs}=1.2V and V_{ds}=1.8V. At output terminal, the reflected RF power stress was done with load reflection coefficient, Γ_L, of 0.351∠-40.33°.

The on-wafer DC characteristics were measured by using an Agilent 4142B Modular DC Source/Monitor at room temperature (T = 300 K). The power measurements were carried out by using Agilent 8241A signal generator and Anritsu ML2438A Power Meter. The Load-Pull measurement for the maximum output power matching was done by MAURY 982B01 tuners. The measurement for the power cells was done at 5.2 GHz.

III. RESULTS AND DISCUSSION

The degeneration degrees of drain current were shown in Figure 2. The device is biased and measured at V_{gs}=1.2V and V_{ds}=1.8V after stress. The drain



current was reduced with the increasing of stress time, because of hot-carrier effects both under DC and RF stresses. After 80 minutes of DC stress, the degradation reached to 4 %. During the RF stress, the load reflection coefficient was set to be 0.351∠-40.33° to establish the load mismatch and three different input power levels was chosen to study the influence of the reflected power on performance degeneration. The degree of degradation from load mismatch after 80 minutes was 9% and 4.5% for input power of 0 and -3 dBm, and 2.1% for input power of -6 dBm. According to measured results shown in Fig. 2, some phenomena are observed. RF load mismatch with high input power induce larger drain current degradation than that of DC stress. The degree of degradation from mismatch depends on the power level.

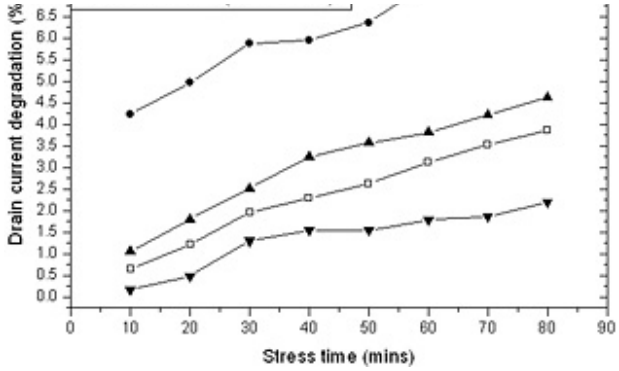
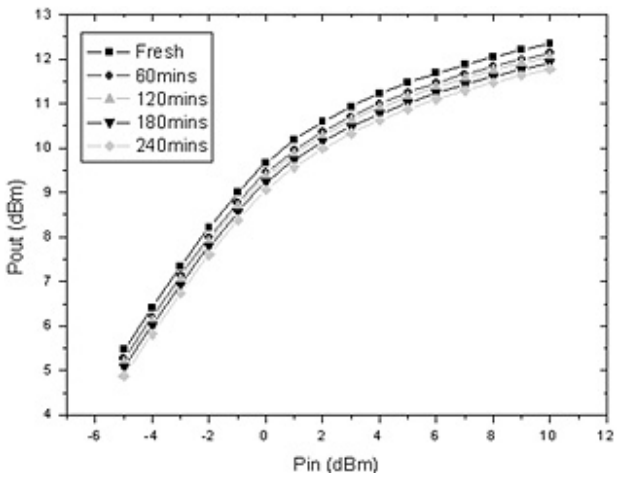


Fig. 2. Comparison of degradations of drain current in RF and DC stresses.(Measured at V_{gs}=1.2 V and V_{ds}=1.8 V)

In this experiment, the reflected power increases the energy of hot carriers. If the energy of electrons and holes overcomes the Si-SiO_2 barrier, the interface states and trapped carriers will occur and cause damage at gate oxide which induces hot-carrier effect[8]. DC stresses resulting from higher V_{gs} and V_{ds} result in more channel carriers and larger channel electric field and then generate more hot carriers. By imposing RF stresses on the output terminal under different input power levels, it is found that the degeneration of drain current after stress is more serious when the reflected power increases. This means that more hot carriers with higher energy will overcome the barrier and induce more damages at gate oxide[8]. Under RF stress, the carriers in channel receive the reflected power from load mismatch. The average energy of each carrier under larger input power is much higher than that from DC stress and results in more hot-carrier injection and then worsens the reliability. But when the input power is small enough, the energy from reflected power may be lower than that from DC stress with high electric field. So the degradation will be mitigated at low input power level.

Figure 3 shows the degradation of output power performances after RF stress with input power of 0 dBm. The output power is degraded from 9.67 dBm to 9.06 dBm after RF stress for 240 minutes. Figure 4 shows the power-added efficiency of the stressed cell. The maximum PAE degraded from 25.77 to 22.78 %. The degeneration was about 3 % after 240 minutes of RF stress. These degradations show a serious influence on the RF power performance of the power cells if the load impedance is not perfect enough and then the equivalent circuit parameters of MOSFET change[6].



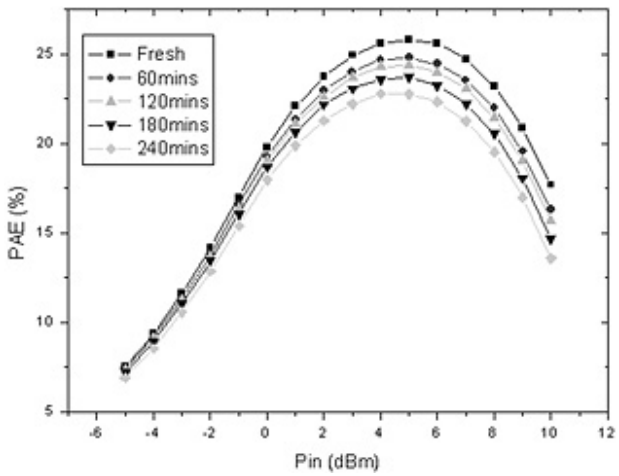


Fig. 3. Degradations of output power with stress time under RF stress at 5.2 GHz.

Fig. 4. Degradations of power-added efficiency with time under RF stress at 5.2 GHz.

Figure 5 shows the shifts of optimum load reflection coefficient for optimum output power in load-pull system. The direction of arrow shows the increase of stress time for 0, 120, and 240 minutes. The optimum load reflection coefficient is 0.2310∠128.6° for the fresh device but it shifts to 0.2453∠125.98° and 0.2753∠121.57° after 120 and 240 minutes of stress, respectively. Because of the damages at the gate oxide near the drain side made by hot carriers and interface states resulting from stresses, the output impedance of MOSFET has been changed [3]. Furthermore, for the optimum power match, the shifts of load reflection coefficient were occurred. These measured results prove that the reflected power indeed affects the characteristics of the cell, especially in the output terminal, drain side.

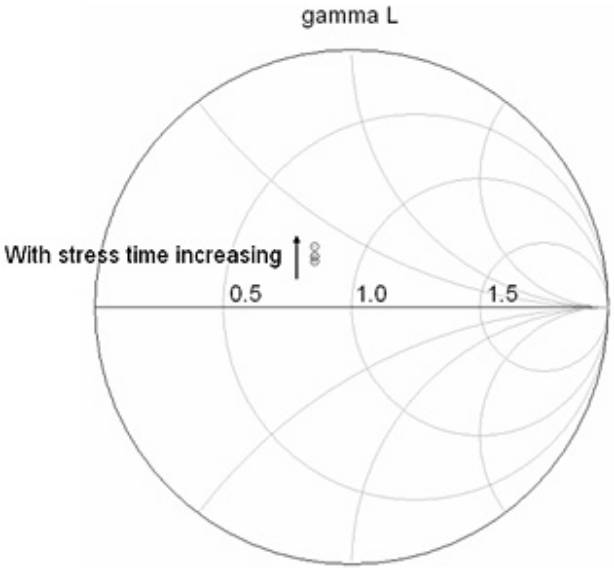


Fig. 5. Shift of optimum reflection coefficient and after RF stress at 5.2 GHz.

It is known that the temperature influences the hot-carrier effect because the fixed positive charge and the interface trap will be significant at high temperature[9]. In this work, the experiment results show the principle that the reflected power also increases the generation of interface states and trapping. Hence, the effect and the degradation from hot carriers are increased. From the measured results of the shift of the optimum power match parameters, it shows that there are some damages near the drain terminal and change the output impedance of the studied cell.

If the impedance of matching network in a power amplifier is changed by the parasitics of passive devices or process variation, the performances of active devices will be influenced by the reflected power from the mismatch of load impedance. The power mismatch issue is important not only on the performances of circuits, but also on the reliability of active devices, especially in high power applications.

The cut-off frequency, f_T, and small-signal gain, S_{21}, were also degraded after the RF stress. The f_T degraded from 62 to 60 GHz and S_{21} degraded from 7.657 to 7.525 dB at 5.2 GHz. Overall, the DC, RF, and power performances will be affected by the hot-carrier effect under load mismatch which is an important issue for circuit designers.

IV. CONCLUSION

In this paper, the effects of load mismatch stress on drain current and RF power characteristics have been presented. The channel width of the studied cell is 5 μm × 16 fingers. The drain current decreased after DC stress with high voltage and RF load mismatch stress. From the measured results, the effect of load mismatch with high input power is more significant than that of DC stress. The measured optimum load reflection coefficient for the maximum output power was changed from the stress. It means that the output impedance of the NMOS was changed because of the hot-carrier effect near the drain side. For RF power performance of the cells, the output power and PAE also degraded. The measured results suggest designers to pay more attentions to the matching networks to improve the reliability of power cells and avoid the degeneration when designing a power amplifier.

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