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A 24/60-GHz CMOS On-Chip Dual-Band Bandpass Filter Using Tri-section Dual-Behavior Resonators

Lung-Kai Yeh, Huey-Ru Chuang*

Institute of Computer & Communication, College of Electrical Engineering and Computer Science, National Cheng Kung University
q3897120@mail.ncku.edu.tw
* chuang_hr@ee.ncku.edu.tw

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I. INTRODUCTION

As the operation frequencies increase, microwave and millimeter waves are applied to broad areas such as vehicular radar systems that provides for the operation of vehicle radar at 24-GHz and 77-GHz [1] or a short range telecommunication band at 60-GHz [2]. In recent years, dual-band filter has been proposed and exploited extensively as a key circuit block in dual-band wireless communication systems. The proposed dual-band bandpass filter using dual-behavior resonators is to operate the system at microwave frequency of 24-GHz in combination with a system that works at a millimeter-wave frequency of 60-GHz. Several novel compact microstrip cross-coupled bandpass filters realized by miniaturized stepped impedance resonators (SIRs) were proposed [3], [4]. The SIRs applied to the dual-band filter design can control second passband by adjusting the impedance ratio and electric lengths of SIRs, as shown in [5]. In [6], skirt selectivity and wide stopband were further enhanced by means of using open-ended $\lambda/4$ stepped-impedance resonators. In addition, stepped-impedance resonators are also applied to the structure of dual-behavior resonators (DBRs). DBRs are composed of the parallel combination of several different open-ended stubs structures. The locations of the transmission zeros in filter design can be achieved [7]. In [8], a high isolation duplexer design with open-circuited dual-behavior resonators (OC-DBRs) used was simply achieved at desired bands. In this paper, RFIC-on-chip 24/60-GHz millimeter-wave CMOS dual-band bandpass filter based on the DBRs structure and SIRs technology is proposed and fabricated. Fig.1. shows the structure of levels of metal in CMOS process and layout of a 24/60-GHz millimeter-wave CMOS dual-band bandpass filter. The compactness of the component's size and the control of the location of two transmission zeros have been demonstrated.

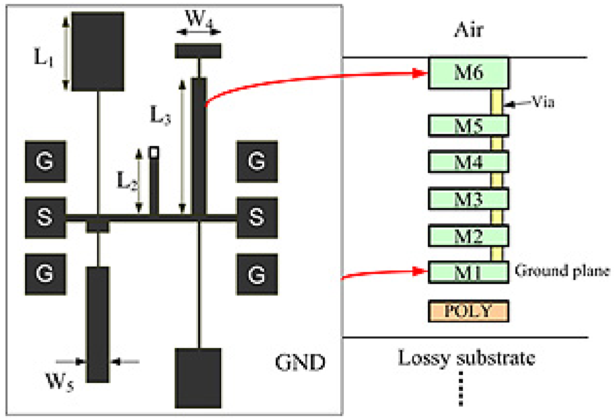


Fig.1. Structure of levels of metal in CMOS process and layout of a 24/60-GHz millimeter-wave CMOS dual-band bandpass filter

II. DESIGN OF DUAL PASSBAND FILTERS

Fig. 2 shows the tri-section stepped impedance resonator with a cascade of different characteristic impedances Z_1, Z_2 and Z_3 and corresponding electrical lengthsθ_1, θ_2 and θ_3. Without the influences of the open-end capacitance and the discontinuity capacitance and inductance, the input impedance, Z_{in}, can be given from [4]. The resonant conditions of the$\lambda/4$ SIR can be obtained by taking $Z_{in}=0$, thus giving

$$\frac{Z_1}{Z_2}\tan\theta_1\tan\theta_2+\frac{Z_2}{Z_3}\tan\theta_2\tan\theta_3+\frac{Z_1}{Z_3}\tan\theta_1\tan\theta_3=1 \quad (1)$$

To simplify the analysis of the tri-section SIR, the definitions of the related ratios $k=Z_1/Z_2$, $m=Z_2/Z_3$ and $\alpha=\theta_2/\theta_1$ are defined first and then substituted into equation (1). The equation (1) can be rewritten as

$$m\tan(\alpha\theta_1)\tan\theta_3+k\tan\theta_1\tan(\alpha\theta_1)+km\tan\theta_1\tan\theta_3=1 \quad (2)$$

The normalized resonator lengthθ_T of the $\lambda/4$ SIR is given by

$$\begin{aligned}\theta_T &= \theta_1+\theta_2+\theta_3\\ &=(1+\alpha)\theta_1+\tan^{-1}\left[\frac{1-k\tan\theta_1\tan(\alpha\theta_1)}{m\tan(\alpha\theta_1)+km\tan\theta_1}\right]\end{aligned} \quad (3)$$

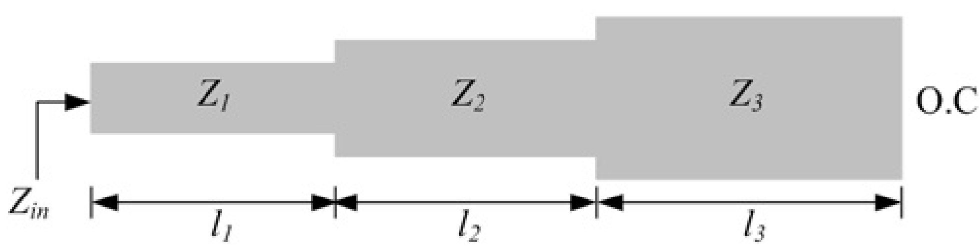
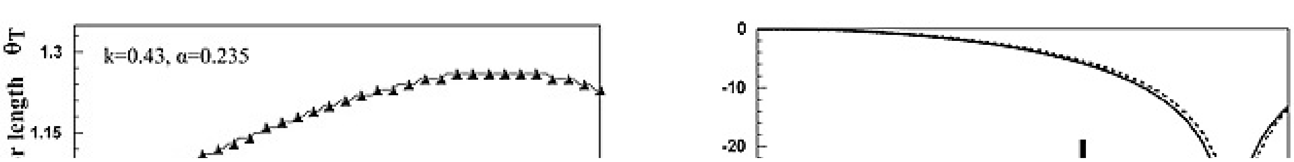


Fig.2. Basic Structure of the tri-section SIR



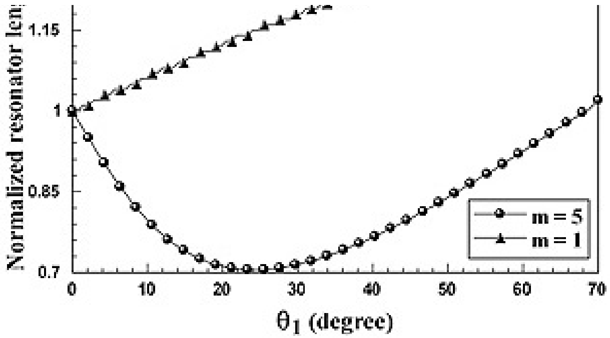


Fig. 3. Normalized resonator length θ_T with different m under the condition of k=0.43 and α=0.235.

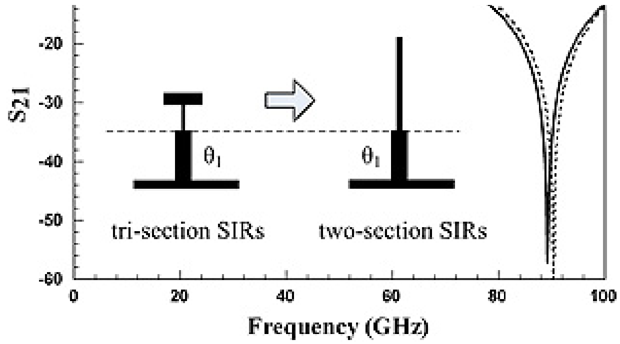


Fig. 4. Resonant frequency equivalency between tri-section SIR and two-section SIR

From Fig. 3, the normalized resonator length θ_T attains a minimum value when the ratio m=5 and a maximum value when the ratio m=1 in the case of setting k=0.43, α=0.235. Here, the ratios of m=5 and m=1 represent tri-section and two-section SIRs, respectively. The overall electric length θ_{T5} (m=5) is apparently smaller than θ_{T1} (m=1) when θ_1 is fixed at 62 degree. As shown in Fig. 4, the designed component's size can be efficiently reduced by replacing two-section SIR with tri-section SIR. By increasing the step number of SIRs, more geometrical parameters are available for design considerations. In Fig. 5, three SIR structures are illustrated. In the cases of the ratio α=3, 4.5, and 6 are simulated for realizing a normalized resonator length θ_T=0.82. The corresponding structure implemented with values of θ_1=12°, 3.2°, and 7.5° are obtained. The DBRs in the design of a 24/60-GHz millimeter-wave RFIC-on-chip dual-band bandpass filter are the combination of two-section and tri-section SIRs structures. Based on the above analysis, the DBRs with different characteristic impedances and electrical lengths can be determined. Each of them contributes one transmission zero on either side of the passband. Fig. 6 shows that the transmission zeros located at 43/93-GHz and 37/92-GHz, respectively. Two different types of OC-DBRs are designed in adjacent resonance frequency, which make the stopband get higher skirt selectivity as well as wider rejection bandwidth. To eliminate the unwanted low-frequency response, a short-circuited stub with *l* < λ/4 is employed for this purpose.

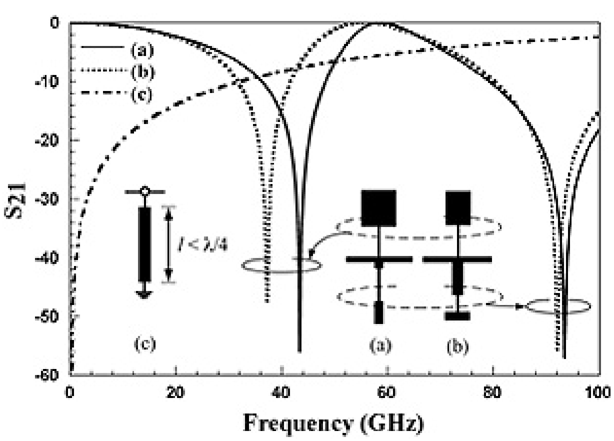


Fig. 5. Normalized resonator length θ_T with different α under the condition of k=0.43 and m=2.34.

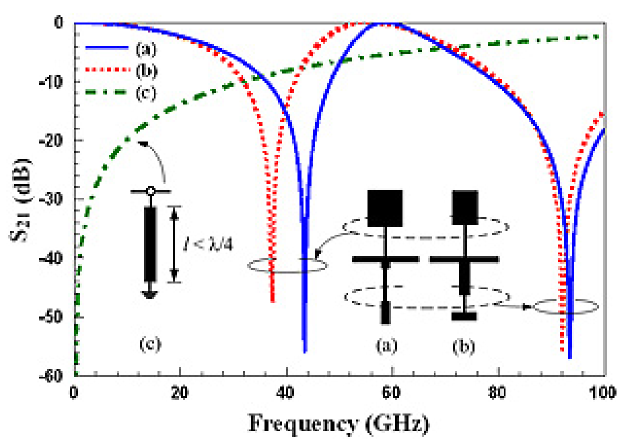
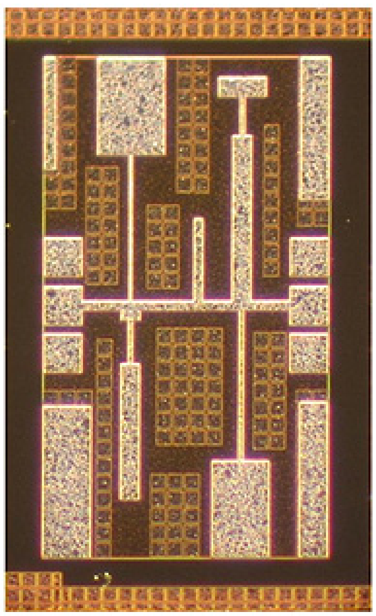


Fig.6. Simulation results of a short-circuited stub and the OC-DBRs with transmission zeros of 43/93-GHz and 37/92-GHz

III. SIMULATION AND MEASUREMENT RESULTS

To demonstrate the application of the studies in the previous sections, a dual-band bandpass filter using stepped-impedance resonators structure and concept of open-circuited dual-behavior resonators is proposed. Fig. 7 shows that the chip micrograph of the designed filter is fabricated on a 0.18-μm CMOS multi-layered structure with a substrate of 500-μm thickness. The millimeter-wave CMOS-based bandpass filter with a low insertion loss was earlier developed by Sun *et al.* [9]. Due to the complexity of a 0.18-μm CMOS multi-layered structure, a way to reduce this complexity is to evaluate effective dielectric constant and simplify it into a single equivalent homogeneous substrate. Based on the formulation [10], the multilayer dielectric constant can be calculated accurately. The dimensionsof the proposed filter are specified as follows: L_1= 0.2 mm, L_2= 0.17 mm, L_3= 0.34 mm, W_4= 0.1 mm, and W_5= 0.04 mm. Without the dummy metal included, the chip size of the proposed filter is 1.03 × 0.590 mm^2. Note that the influences of the open-end capacitance and the discontinuity capacitance and inductance will result in the location of stopband to be shifted to the lower frequency. The rejections in the stopbands are all lower than -20-dB. The filter with lower resonant frequency of 24-GHz has less than 3.6-dB insertion loss and greater than15-dB return loss, the second passband with center frequency of 60-GHz has less than 2.8-dB insertion loss and greater than 10-dB return loss. The S-parameter simulation and measurement results for designed filter are shown in Fig. 8.



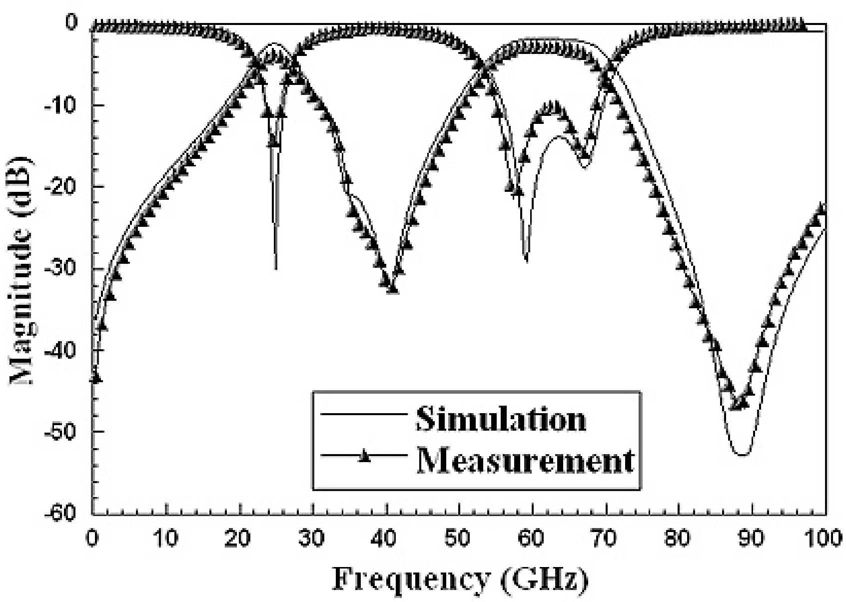


Fig. 7. Chip microphotograph (Left).
Fig. 8. S-parameter simulation and measurement results of the designed millimeter-wave CMOS dual-band bandpass filter (right).

This paper presents the design and implementation of a 24/60-GHz millimeter-wave CMOS dual-band on-chip bandpass filter using a 0.18-μm standard CMOS process. A method based on the concept of dual-behavior resonators has been investigated and implemented. Tri-section SIRs with more geometrical parameters not only reduce the chip's size, but also increase the flexibility of design. The 24/60-GHz dual-band bandpass filter is illustrated and measured. The measurement results are found to be in good agreement with the simulation results.

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