English
Research Express@NCKU Volume 8 Issue 3 - April 3, 2009
[http://research.ncku.edu.tw/re/articles/e/20090403/3.html]

Effect of hot-carrier-induced interface states distribution on linear drain current degradation in 0.35 um n-type lateral diffused metal-oxide-semiconductor transistors

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Applied Physics Letters, Vol. 92, pp. 103510, March 2008

High-voltage lateral diffused MOS (LDMOS) transistors are widely used in smart power applications because they are easily to be integrated into standard CMOS process. Because of relatively high operational voltages, LDMOS transistors are prone to hot-carrier-induced degradation. The investigation of the mechanism of hot-carrier-induced linear drain current (I_{dlin}) degradation (increase of on-resistance) is necessary because transistors with a lower on-resistance produce smaller power consumption. To evaluate this concern, this work presents the mechanisms of hot-carrier-induced I_{dlin} degradation in n-type LDMOS devices.

Devices investigated in this study are n-type LDMOS transistors fabricated by a 0.35 μm CMOS process. Figure 1(a) shows schematic cross-section of the device. The p-type channel region (L_{ch}), n-type accumulation region under poly-gate (L_{acc}), and drain side spacer region (L_{sp}) are indicated in the figure. Gate oxide thickness of the device is 30 nm and poly-gate length is 0.8 μm. Operational voltage for both drain voltage (V_{ds}) and gate voltage (V_{gs}) is 12 V. To evaluate the damage created by hot carriers, stressing under V_{ds} = 13.2 V and various V_{gs} ranging from 3 to 11 V for 3000 seconds is performed at room temperature. I_{dlin} is measured under V_{ds} = 0.1 V and V_{gs} = 12 V. Threshold voltage (V_{th}) is extracted under V_{ds} = 0.1 V using maximum transconductance method. During stressing, I_{dlin}, V_{th}, and charge pumping current (I_{CP}) are monitored periodically. I_{CP} is measured to extract stress-induced interface state density (ΔN_{it}). Figure 1(b) shows the experimental setup of charge pumping measurement performed in this work. The pulse in charge pumping measurement is applied to the gate while drain and bulk terminals are grounded. The source terminal is floating. The amplitude of the pulse is fixed at 10 V and base voltage (V_{base}) sweeps from -8 to 2 V under a frequency of 500 kHz. Process (TSUPREM4) and device (Medici) simulations are also performed to investigate the mechanism of hot-carrier-induced degradation.

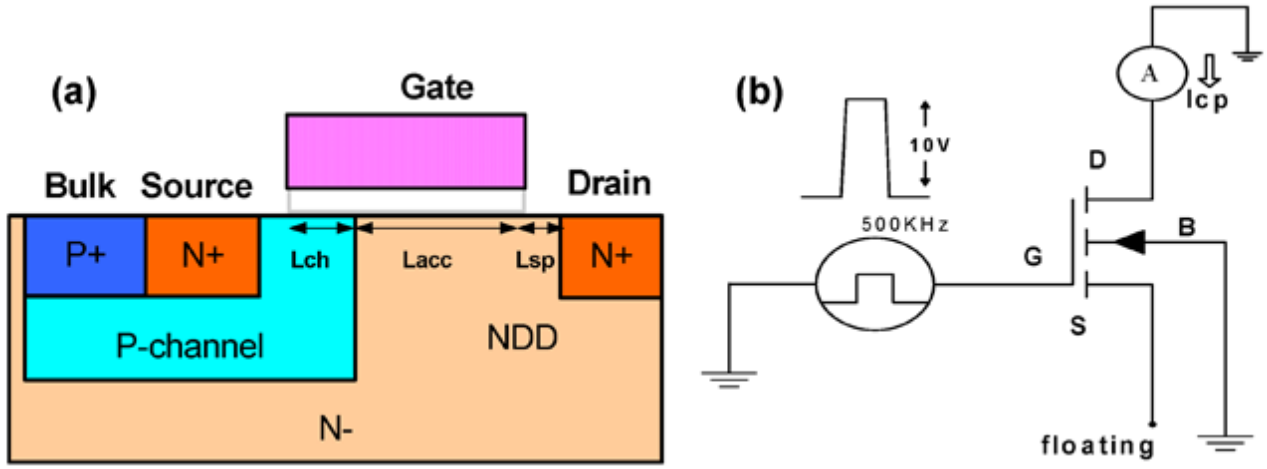

Fig. 1. (a) Schematic cross-section of the n-type LDMOS device used in this work. (b) The experimental setup of charge pumping measurement.

Figure 2(a) shows I_{dlin} degradation and V_{th} shift as a function of stress time for devices stressed under V_{ds} = 13.2 V and V_{gs} ranging from 3 to 11 V. Results show that higher V_{gs} produces more I_{dlin} degradation. For devices stressed under V_{gs} = 3 to 9 V, V_{th} shift is little (< 5 mV), indicating that hot-carrier-induced damage located in L_{ch} region is small. Most of the damage is located in L_{acc} and L_{sp} regions. However, V_{th} shift is more than 10 mV when the device is stressed under V_{gs} = 11 V, revealing that damage location moves into L_{ch} region. Bulk current (I_b) vs. V_{gs} characteristics under various V_{ds} is shown in Fig. 2(b). It is clear that Kirk effect is not significant in our LDMOS device because I_b does not increase at high V_{gs} (V_{gs} = 12 V). Thus, the impact of Kirk effect on device degradation is not taken into consideration in the following analysis.

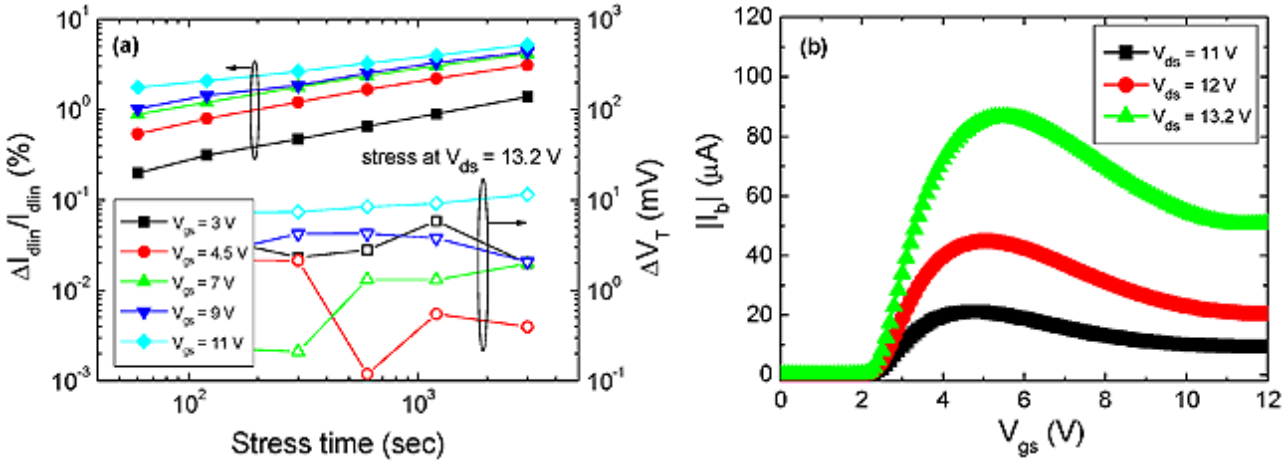

Fig. 2. (a) I_{dlin} degradation and V_{th} shift as a function of stress time for devices stressed under V_{ds} = 13.2 V and V_{gs} ranging from 3 to 11 V. (b) I_b vs. V_{gs} characteristics under various V_{ds}.

To investigate the degradation mechanism, Fig. 3 analyzes stress-induced increase in I_{CP} (ΔI_{CP}) for the devices shown in Fig. 2(a) stressed for 3000 seconds. The location dependent V_{th} and flat band voltage (V_{fb}) obtained from TCAD simulations are investigated and the results are shown in Fig. 4. Based on V_{th}

and V_{fb} distributions obtained in Fig. 4, ΔI_{CP} measured at V_{base} = -8 V is proportional to total ΔN_{it}, i.e., ΔN_{it} in L_{ch}, L_{acc}, and L_{sp} regions. Similarly, ΔI_{CP} measured at V_{base} = -2 V is proportional to ΔN_{it} located in L_{ch} and L_{acc} regions, while ΔI_{CP} measured at V_{base} = 0.5 V is proportional to ΔN_{it} located in L_{ch} region only. According to the above analysis, little ΔI_{CP} is observed at V_{base} = 0.5 V for devices stressed under V_{gs} = 3 to 9 V, indicating that hot-carrier-induced ΔN_{it} is mainly distributed in L_{acc} and L_{sp} regions. As the stress V_{gs} is increased to 11 V, significant ΔI_{CP} is observed at V_{base} = 0.5 V, suggesting that significant ΔN_{it} is created in L_{ch} region.

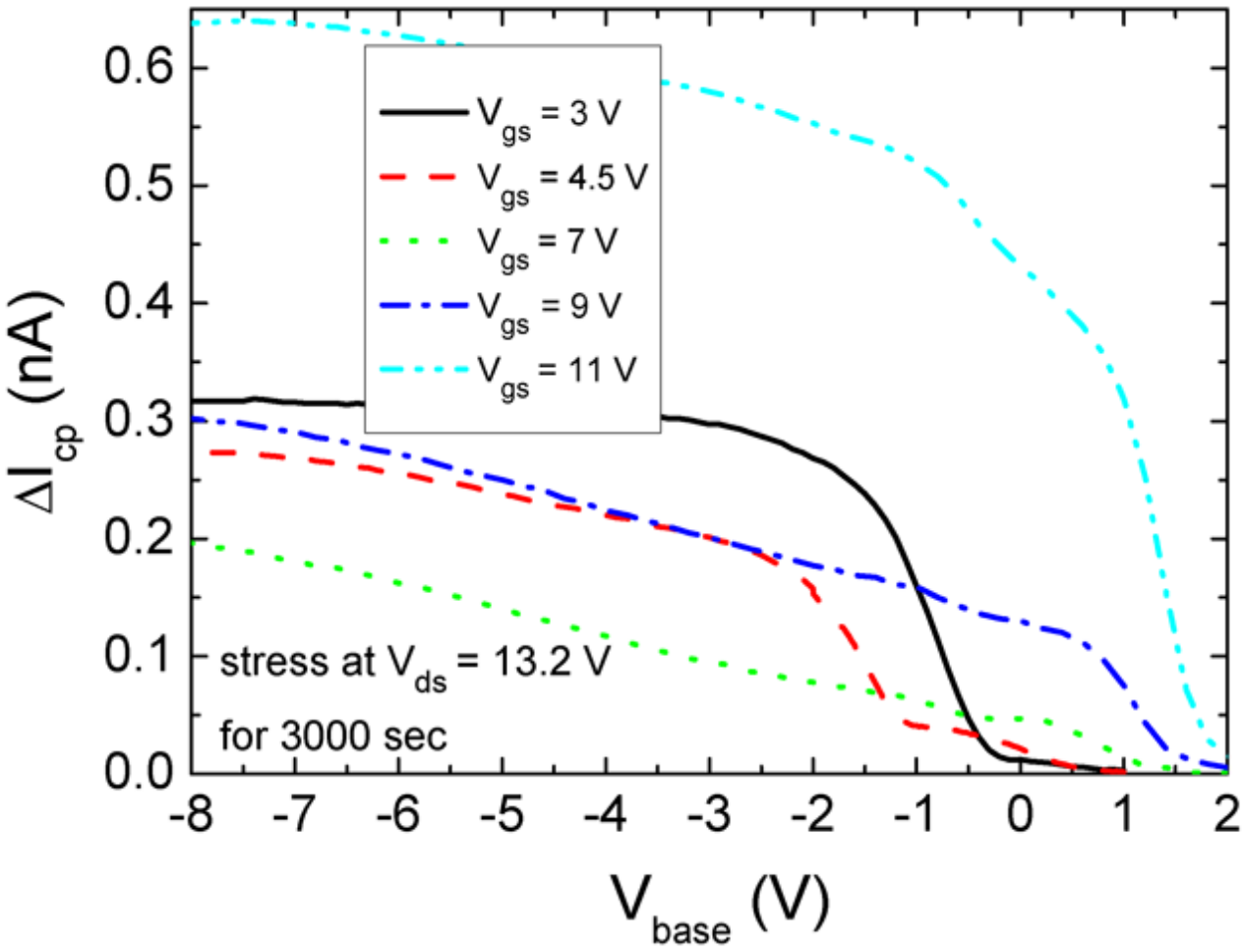

Fig. 3. Stress-induced ΔI_{CP} as a function of V_{base} for the devices shown in Fig. 2(a) stressed for 3000 seconds.

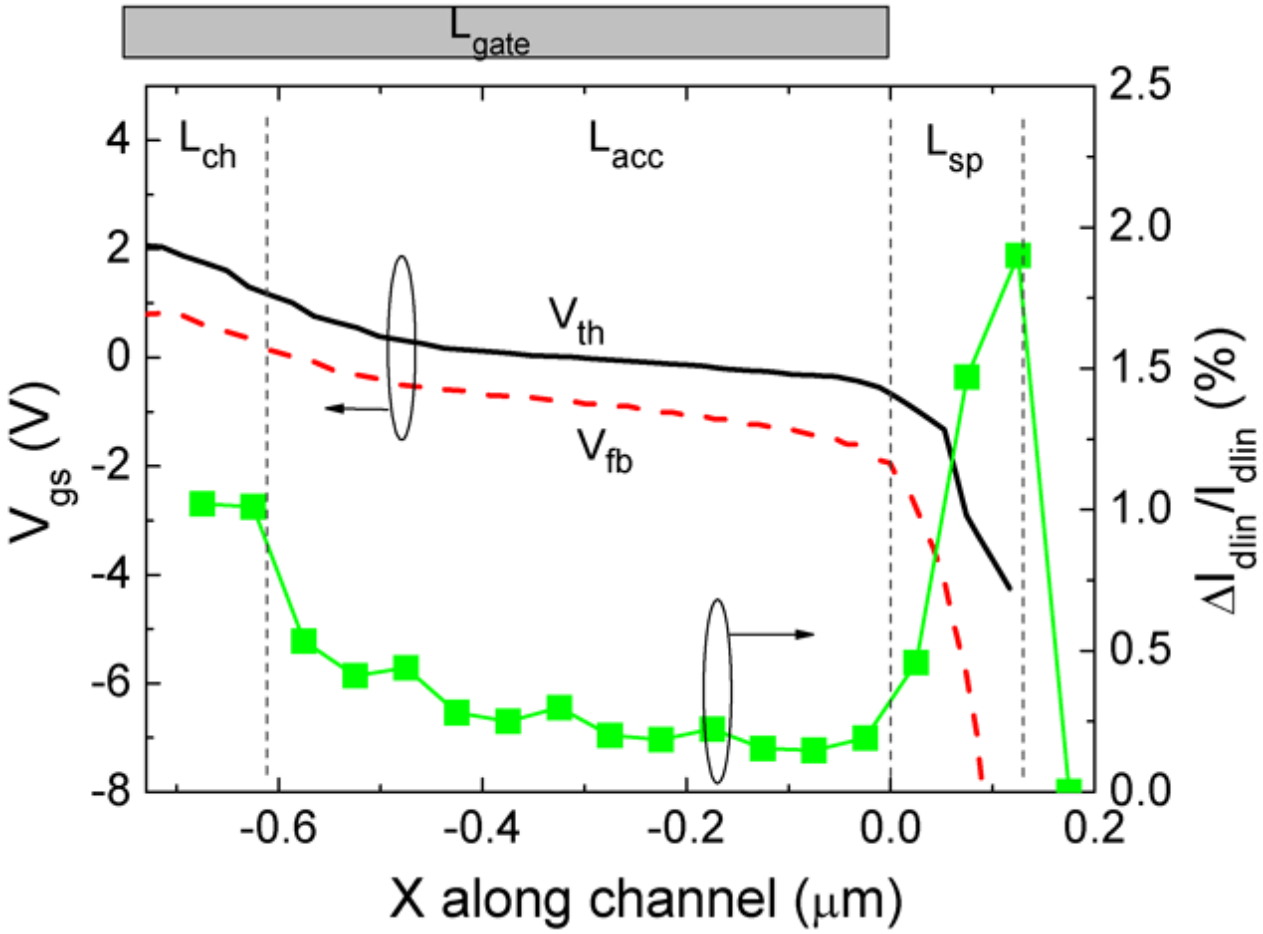

Fig. 4. Location dependent V_{th} and V_{fb} as well as I_{dlin} degradation resulted from ΔN_{it} at different locations are simulated.

Since ΔN_{it} is located at various regions, the impact of damage location on I_{dlin} degradation should be examined. This can be achieved by TCAD simulations. The same amount of interface states distributed in a range of 0.05 μm but centered in different locations are assigned from channel to spacer edge in simulations. I_{dlin} degradation resulted from interface states at different locations are shown in Fig. 4. Results reveal that interface states in L_{sp} region produce the most I_{dlin} degradation. Interface states in L_{ch} region also degrade I_{dlin} but not as much as that of damage in L_{sp} region. Interface states in L_{acc} region produce the least I_{dlin} degradation. To confirm the above argument, Fig. 5 shows the relationship between device I_{dlin} degradation and the average interface states density in spacer region (ΔN_{it_sp}). For devices stressed under V_{gs} = 3 to 9 V, a unified relationship between I_{dlin} degradation and ΔN_{it_sp} is obtained. For the device stressed at V_{gs} = 11 V, larger I_{dlin} degradation is observed because ΔN_{it} in L_{ch} region also contributes to I_{dlin} degradation. Results in Fig. 5 confirm that when ΔN_{it} in L_{ch} region is negligible, ΔN_{it} in L_{acc} region is not an important factor and only ΔN_{it} in L_{sp} region dominates the I_{dlin} degradation.

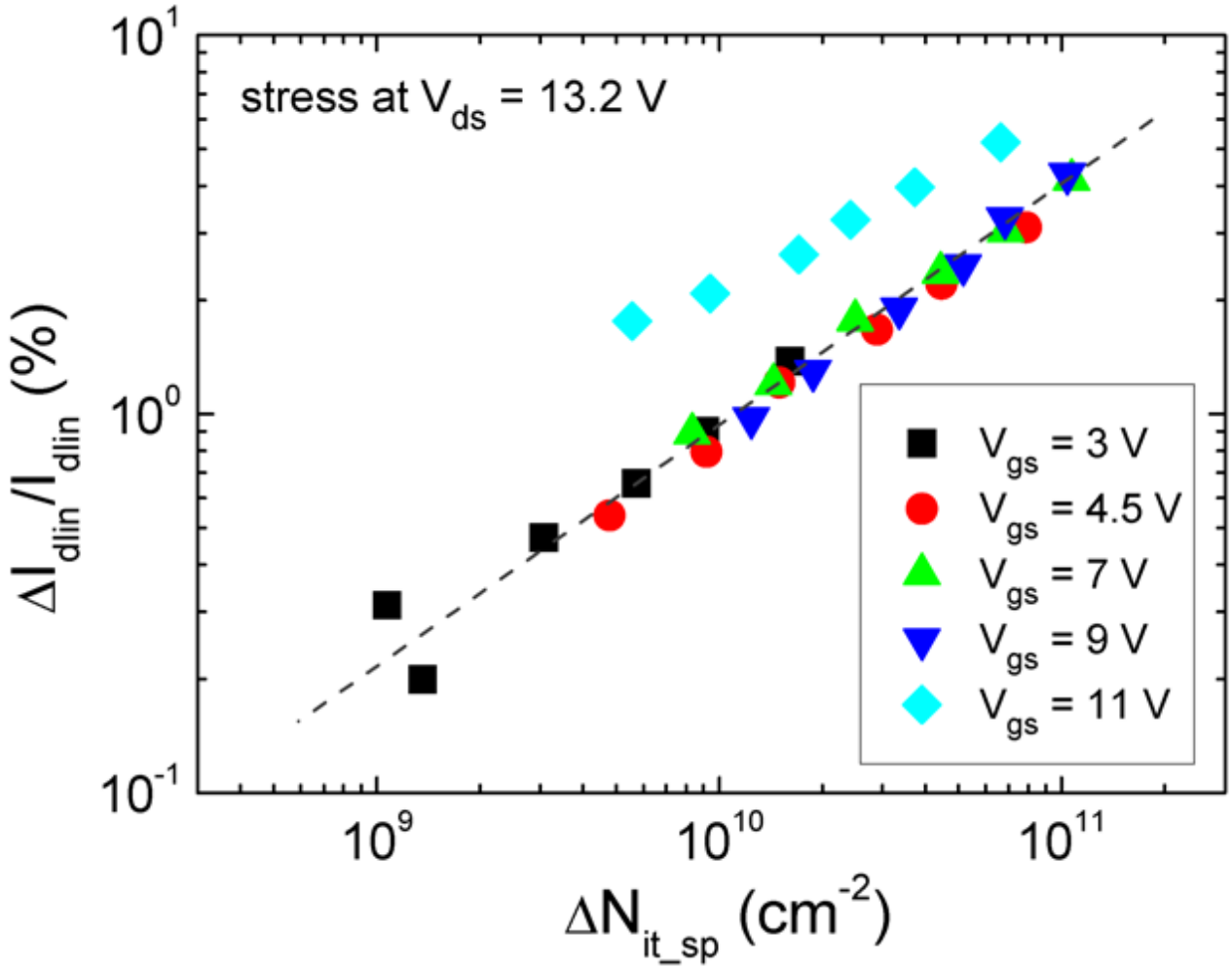

Fig. 5. Relationship between I_{dlin} degradation and average ΔN_{it} in L_{sp} region is shown.

In conclusion, mechanisms of hot-carrier-induced I_{dlin} degradation in our n-type LDMOS transistor have been presented. The device degradation is mainly caused by hot-carrier-induced ΔN_{it}. Experimental data and TCAD simulations reveal that ΔN_{it} located in L_{acc} region has little effect on I_{dlin} degradation, while ΔN_{it} located in L_{sp} region has great impact on I_{dlin} degradation. According to the results presented in this study, not only the magnitude of total hot-carrier-induced ΔN_{it} but also the location of ΔN_{it} should be considered in evaluating LDMOS transistors' reliability.