English
Research Express@NCKU Volume 6 Issue 9 - December 5, 2008
[http://research.ncku.edu.tw/re/articles/e/20081205/5.html]

Dynamic Negative Bias Temperature Instability (NBTI) on Low-Temperature Polycrystalline Silicon (LTPS) Thin Film Transistors

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IEEE Electron Device Letters, Vol. 29, No. 5, pp. 477-479, May 2008.

The low-temperature poly-Si thin film transistors prepared on glass substrates (LTPS TFTs) have been studied extensively for active matrix liquid crystal display applications. Comparing to the amorphous silicon TFTs (a-Si TFTs), the LTPS TFTs have several orders of magnitude higher electron mobility. In addition, it is possible to integrate the LTPS TFTs with peripheral circuits on same glass substrate for advanced flat panel display applications. Thus, the reliability of LTPS TFTs such as negative bias temperature instability (NBTI) now becomes important and necessary. In the past, the NBTI characteristics of LTPS TFTs were evaluated with the conventional static measurements. However, the recovery issue in static NBTI measurements resulted in an incorrect estimation of life time as has been found in a dynamically operated CMOS device. Hence, the investigations of NBTI with dynamic stress are indispensable. Nevertheless, so far, the study of dynamic NBTI of LTPS TFTs has not been reported. In this paper, for the first time, the behaviors and mechanisms of the dynamic NBTI on LTPS TFTs were investigated in details.

Figure 1 shows the negative threshold voltage shift ($-\Delta V_{th}$) as a function of stress frequency under static and dynamic NBT stress, respectively. For fair comparison, the effective stress time of static and dynamic NBT stress was set equal, i.e. 1000 sec and 500 sec for dynamic and static stress, respectively. Severer degradations were observed for both static NBT stress and low frequency dynamic stress. In addition, the negative shift of threshold voltage under dynamic NBT stress decreases gradually with increasing frequency. This frequency dependence of dynamic NBTI on LTPS TFTs is quite different to the frequency-independent observed on conventional MOSFETs. Because, in the MOSFET, the NBTI is mainly attributed to the generation of interface states, but the time for effective stress and recovery in the dynamic stress is equal, thus the generation of interface states (N_{it}) under dynamic NBT stress is independent of stress frequency

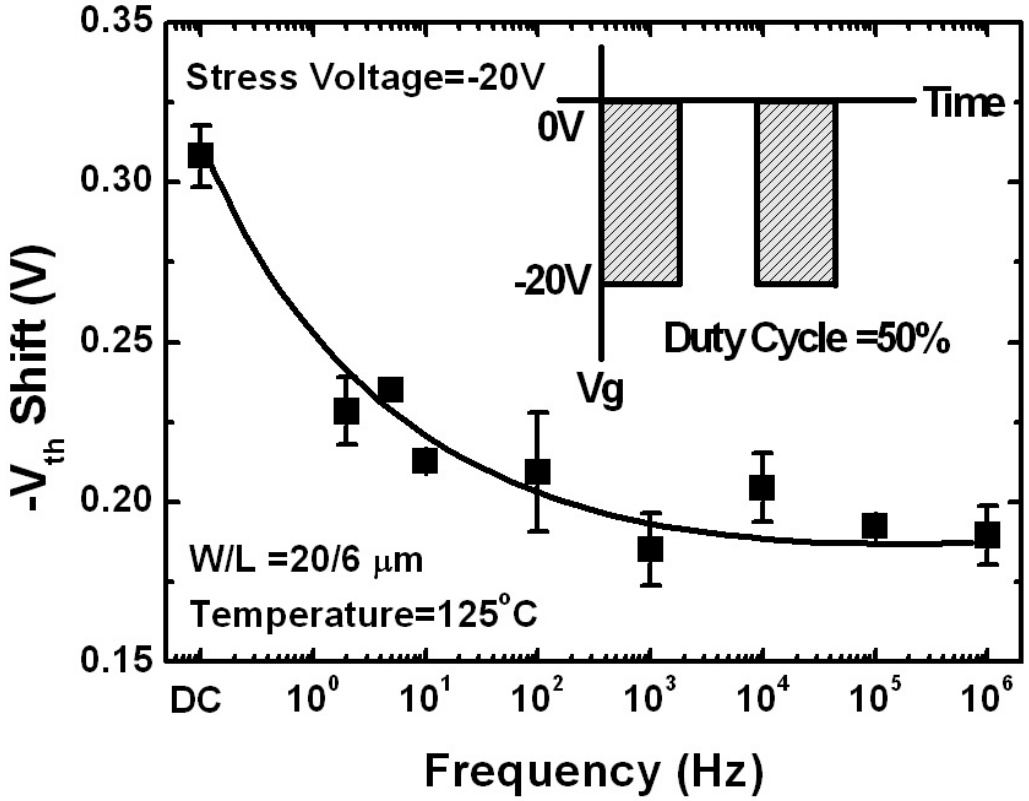

Fig.1. The negative threshold voltage shift ($-\Delta V_{th}$) under static and dynamic negative bias temperature stress Vs stress frequency.

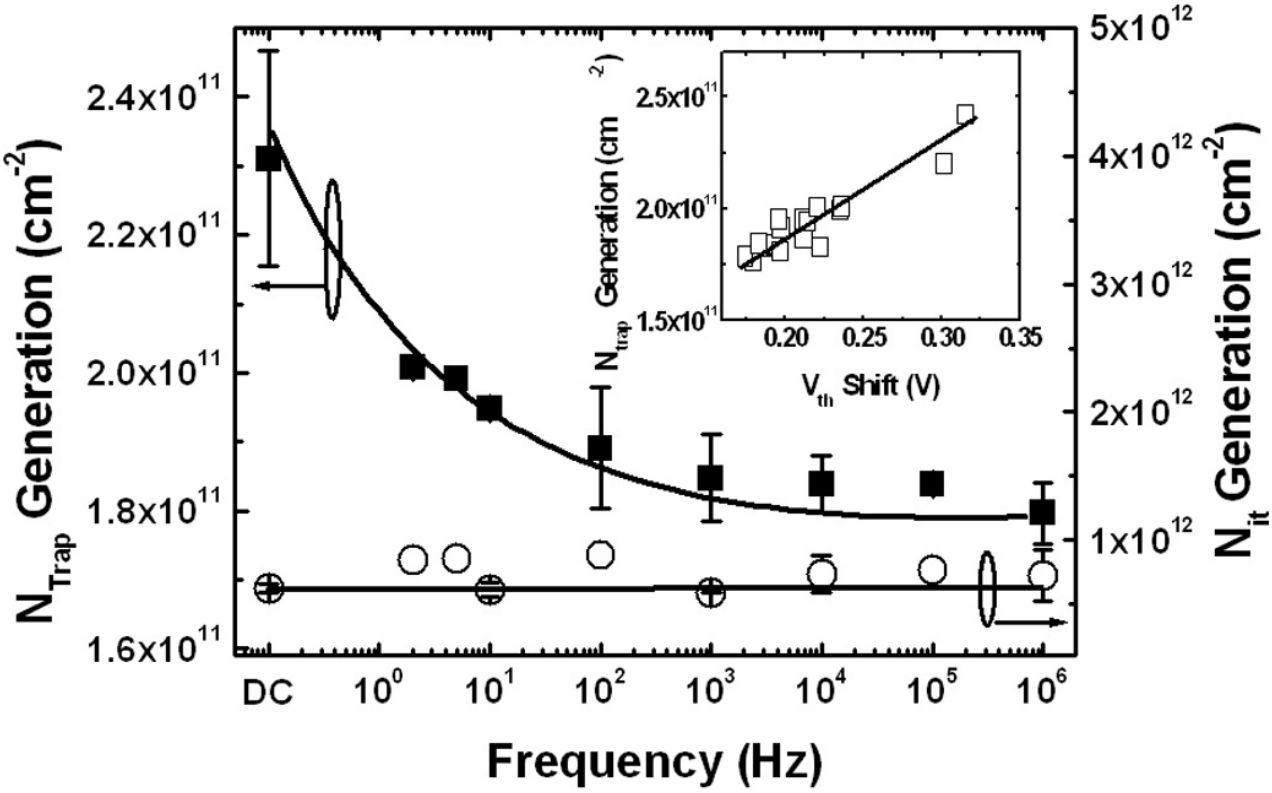

Fig. 2. The generation of N_{Trap} (square) and N_{it} (circle) under static and dynamic NBT stress as a function of stress frequency.

Figure 2 shows N_{Trap} after static and dynamic NBT stress as a function of stress frequency. N_{Trap} was extracted from the measurement of driving current (Id) versus gate voltage (Vg) based on Levinson and Proano method. Obviously, N_{Trap} has similar frequency dependence behavior as that in $-\Delta V_{th}$ (Fig. 1). It is worthy to note that the generation of N_{Trap} has a strong correlation to the $-\Delta V_{th}$ as inserted in Fig. 2. In addition, Fig. 2 also shows the generated N_{it} after static and dynamic NBTI stress as a function of stress frequency. The N_{it} was extracted from the sub-threshold swing (S.S.) by neglecting the depletion capacitance in active layer according to the following equation,

$$N_{it} = \left[\left(\frac{S}{\ln 10}\right)\left(\frac{q}{kT}\right) - 1\right]\left(\frac{C_{ox}}{q}\right), \qquad (1)$$

, where q, K, T, and C_{ox} are electron charge, Boltzmann constant, temperature, and gate dielectric capacitance, respectively. As seen, the Nit generation of LTPS TFTs under dynamic NBT stress is independent of stress frequency. Thus, based on Figs. 1 and 2, the generation of N_{Trap} in poly grain boundary dominates the dependence of frequency after dynamic NBTI stress for the LTPS TFTs.

Furthermore, the behaviors of traps generation in grain boundary during dynamic stress was investigated with capacitance-voltage (C-V) measurements under various frequencies for the LTPS TFTs with gate area of 1000 μm^2 as shown in Fig. 3. As frequency decreasing, C-V curves are shifted in the direction of positive bias, and a plateau is found in the C-V curve at very low frequency (1k Hz). Fig.4 presents the scheme to illustrate the reactions between hydrogen atoms and carriers in the channel. Under high frequency, only the inversion charges at Si/SiO_2 interface can immediately follow the measuring frequency for the longer transit time of grain boundary traps than that of holes in the valence band. However, as the frequency is lowered to 1 k Hz, holes can be generated both at interface and grain boundary. Thus, the additional carriers located at grain boundaries shift the C-V curves and induce a plateau in the low frequency C-V curve. We suspect the plateau in LTPS TFT is come from the carrier confinement in grain boundary traps, thus, the apparent carrier concentration (N_{appl}) including all types of electrically active carriers can be extracted similarly by C-V curves based on the equation 2,

$$\frac{1}{N_{appl(LF)}(V_G)} = \frac{q\varepsilon_{Si}}{2}\frac{\partial\left(\frac{1}{C^2_{LF}}\right)}{\partial V_G} \qquad (2)$$

,where εSi, and C_{LF} are the permittivity of Si and the capacitance measured under low frequency, respectively. Vg is the gate voltage. The N_{appl} of LTPS TFTs extracted from Fig. 3 and based on the equation is shown in the inset of Fig. 3 as a function of gate bias for various frequencies. At high frequency, only one turning point ($V_{T,\,500k\,Hz}$) corresponded to the threshold voltage of the inversion holes at Si/SiO_2 interface is observed. At low frequency, two discrete turning points corresponded to the inversion holes at Si/SiO_2 interface ($V_{T,\,1k\,Hz}$) ,and at grain boundary trap states ($V_{T,\,GB}$) away from interface respectively, are observed as indicated by arrows. Therefore, larger quantity of inversion holes in the grain boundary trap states are expected for the enough response time. These inversion holes under static and lower frequency dynamic stress react with S-H bonds to generate grain boundary traps, consequently, according to R-D model, the trap from NBTI stress increase with the increasing inversion holes. However, the number of inversion holes at Si/SiO_2 interface with faster response time is

insensitive to frequency, thus the interface states generated by the interface holes is regardless of dynamic stress frequency as shown in Fig. 2.

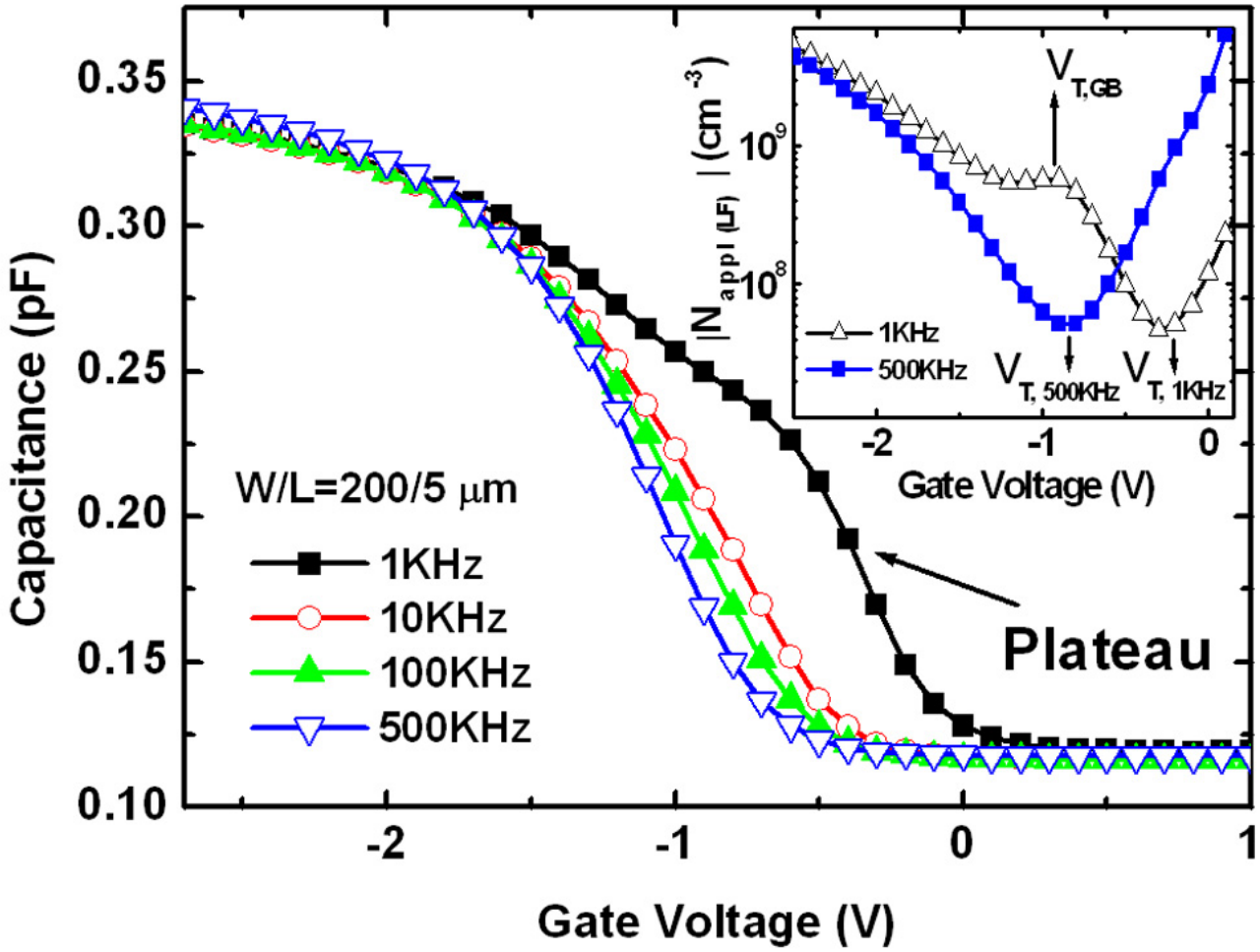

Fig. 3. The C-V characteristics of the LTPS TFTs. The inset shows the N_{appl} Vs gate bias.

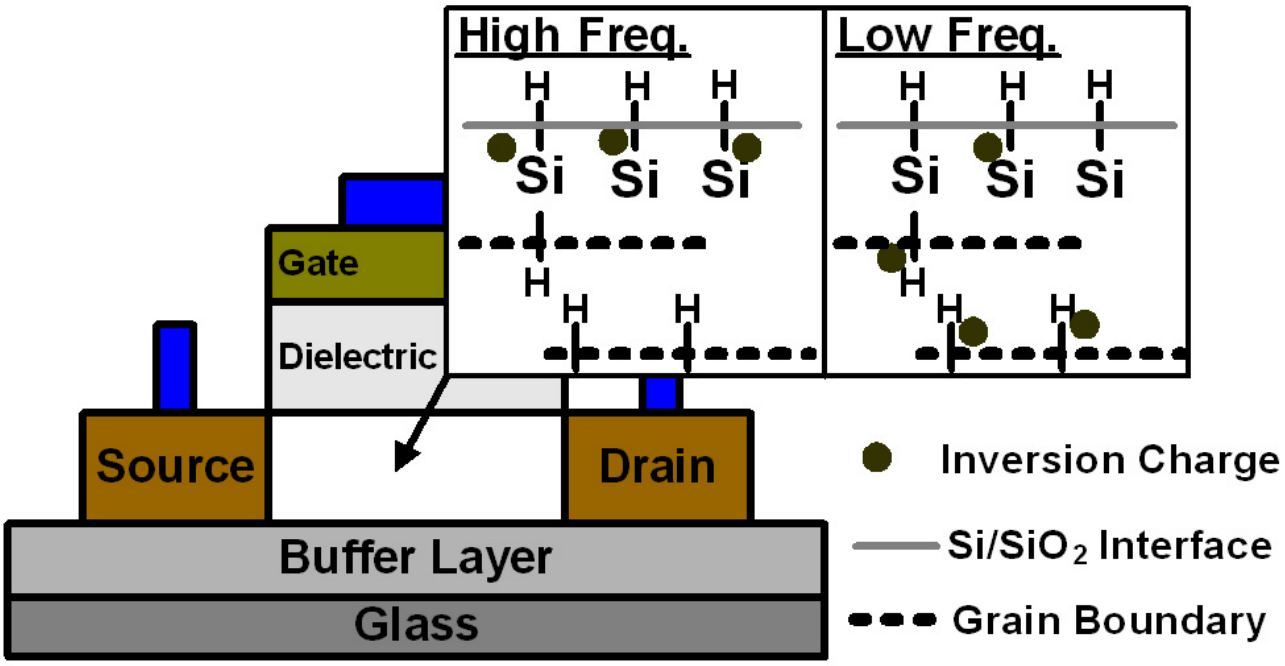

Fig. 4. Schematic diagram of LTPS TFT cross-section, and interaction between hydrogen atoms and inversion charges

In summary, dynamic NBTI characteristics on LTPS TFTs different to the conventional MOSFETs were observed. The NBTI degradations increased with decreasing frequency of dynamic NBT stress. The frequency dependence was attributed to both larger quantity of grain boundary traps and its slow inverse transit time. Thus, to precisely evaluate the life time of LTPS TFTs under AC operation, only the conventional static measurement is insufficient, and the dynamic NBTI reliability tests is indispensable.