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A 60-GHz Millimeter-Wave CPW-Fed Yagi–Antenna Fabricated Using 0.18-µm CMOS Technology

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I.INTRODUCTION

Recently, there exists an increasing demand for broadband multimedia applications for an ever-increasing capacity of wireless networks. In particular, for dense local communications, the 60- GHz band for wireless personal area network (WPAN) applications is of special interest to the short range communications due to its attenuation characteristic of atmospheric oxygen of 10 to 15 dB/km in a band-width of about 8 GHz centered around 60 GHz. It makes the 60-GHz band becomes an attractive alternative for the short-range wireless communications [1]. In order to pursue the RF system-on-chip (SoC) for the 60-GHz radio and the antenna integrated with low-cost monolithically integrated CMOS RF front-end circuitry, millimeter-wave CMOS RFICs and on-chip antenna have been studied [2]-[4]. In 2006, Zhang *et al.* have proposed an on-chip inverted-F antenna fabricated on a low-resistivity silicon substrate [5]. In this paper, a 60-GHz CMOS on-chip CPW-fed Yagi antenna is presented. The on-chip antenna is fabricated with a 0.18-µm CMOS process. Various designs of the planar PCB CPW-fed quasi-Yagi antenna has been reported the X-band which use a ground plane acting as a reflector [6], [7]. In our design, the 0.18 µm 6-metal-layer CMOS process (see Fig. 1) allows the on-chip antenna to utilize a simple CPW to CPS feed transition [8] and the first metal-layer to implement a reflector strip. This on-chip antenna design alleviates the complicated feeding network commonly required for the design of quasi-Yagi antenna. The HFSS FEM-based 3-D full-wave EM solver is used for the design simulation. The on-wafer measurement in a microwave probe station is conducted to measure the input SWR and the antenna power gain of the designed on-chip antenna.

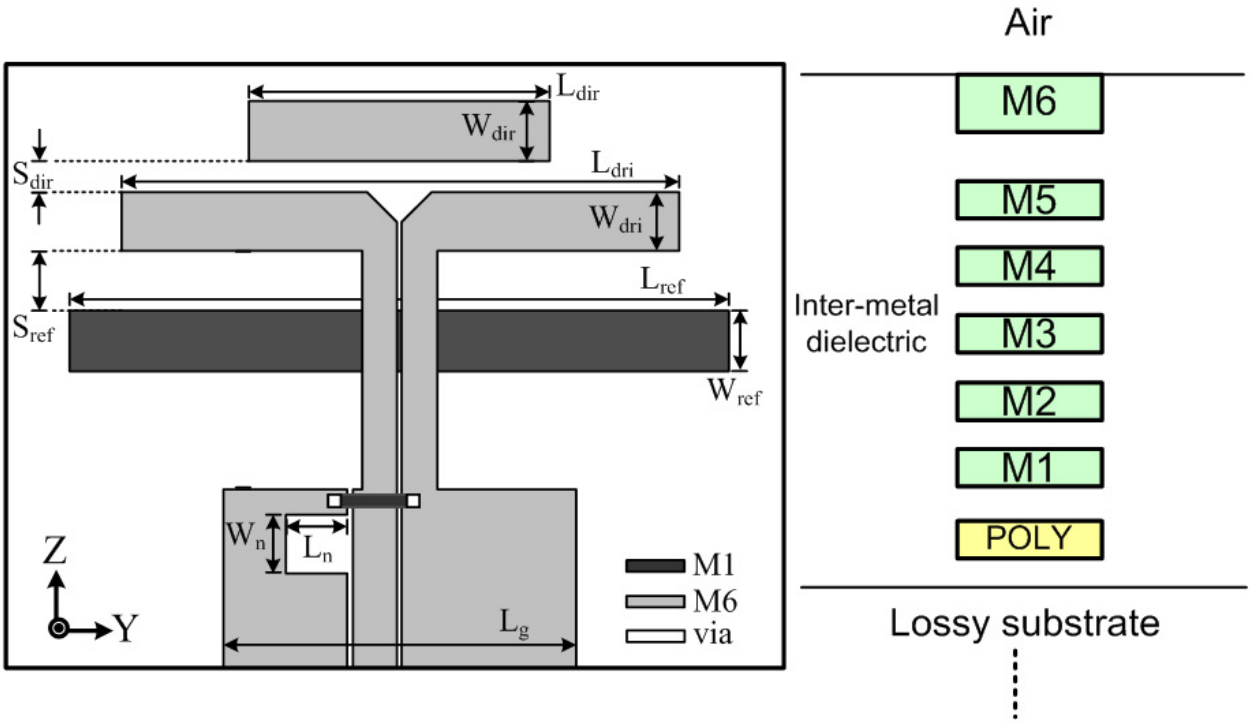

Fig.1 Schematics and cross-sectional view of the designed 60-GHz CPW-fed Yagi CMOS on-chip antenna.

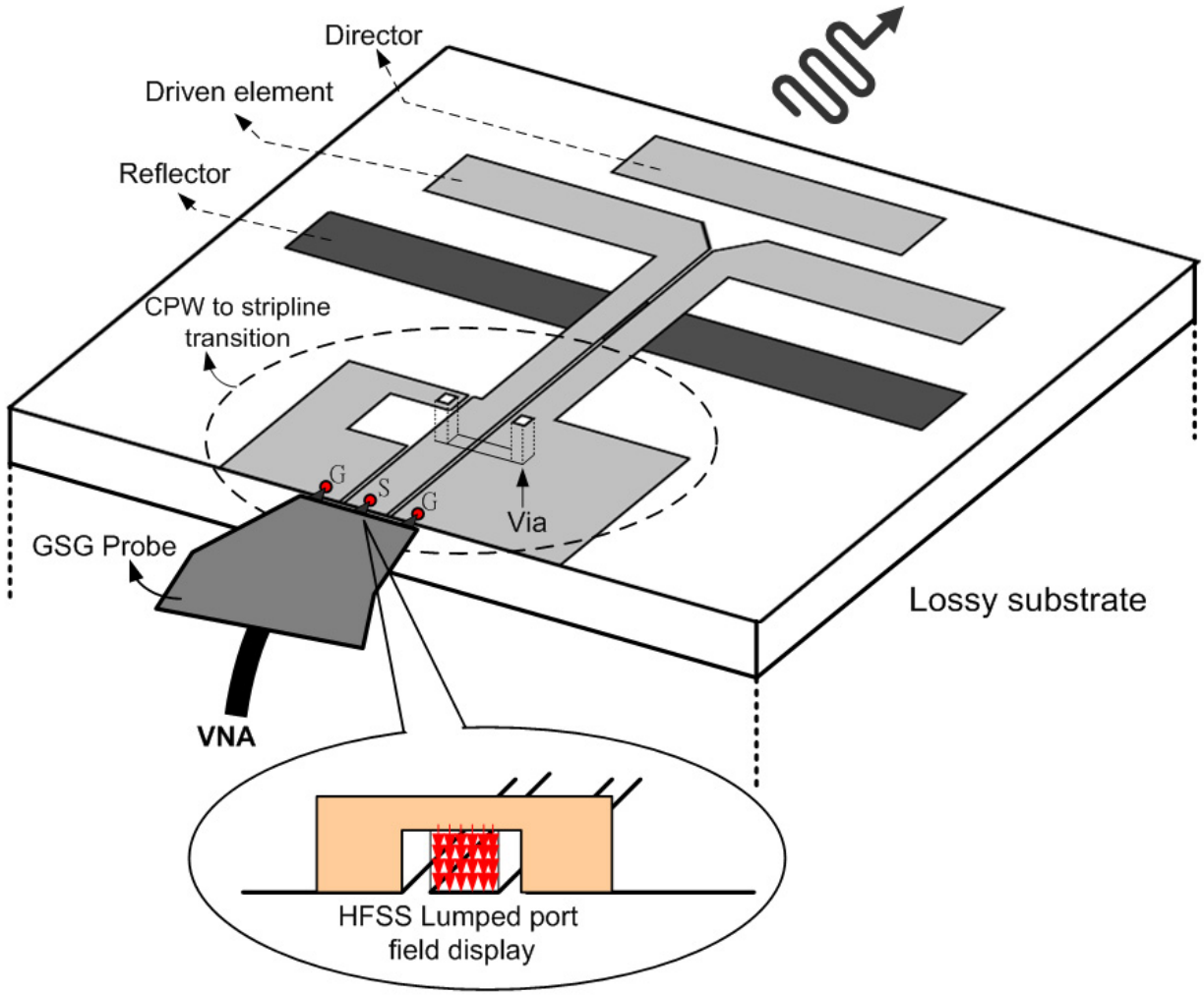

Fig.2 Illustration of HFSS port excitation of the on-chip antenna.

II.ANTENNA DESIGN

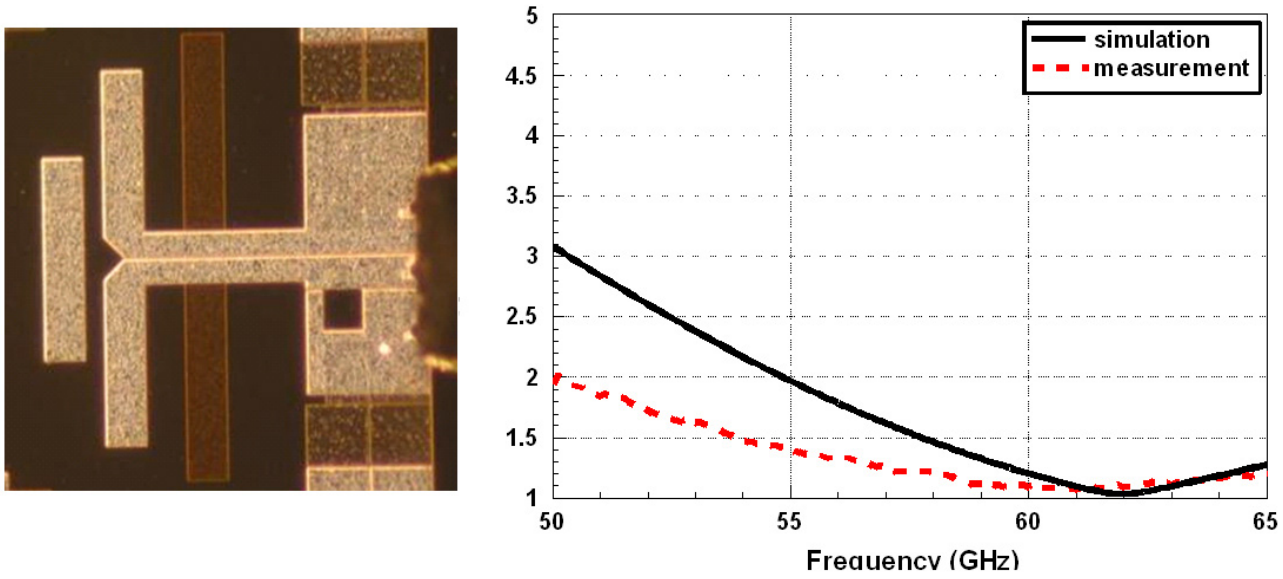

Fig.3 (a) CMOS antenna chip micrograph. (b) Simulated and measured antenna input SWR

A schematic of the proposed CMOS on-chip antenna is shown in Fig. 1. The antenna consists of a director element, a driven element, a reflector element and a ground plane. Except the reflector element is on the first-metal-layer (M1), all others are on the sixth-metal-layer (M6). As shown in Fig. 2, a transition is used to convert the CPW mode at the input to the CPS mode feeding the driven element. The figure also illustrates the HFSS port excitation of the on-chip antenna. The radiation boundary condition is applied in the HFSS simulation. One slot line in the CPW is terminated by open circuit and an air-bridge (M1 and via16) connects the two strips of CPW. The air-bridge can keep two ground planes at the same potential [8], [9]. The length of the driven element, the director and reflector elements should be around $0.5\lambda_{eff}$, $0.45\lambda_{eff}$ and $0.6\lambda_{eff}$ according to the Yagi design principles [10]. Here, λ_{eff} is the effective wavelength calculated by assuming the following value for the effective dielectric constant of the substrate; $\varepsilon_{eff} = (\varepsilon_r+1)/2$, [11], [12], where ε_r is the dielectric constant of the silicon substrate. Table I listed the antenna dimensions.

TABLE I PERFORMANCE SUMMARY

	Simulation	Measurement
Frequency range (GHz)	55–65	55–65
VSWR	< 2	< 2
Radiation efficiency	10 %	-----
Max. antenna power gain (dBi)	-8	-10.6
Front-to-back ration (dB)	9	-----
Chip size	1.1 × 0.95 mm^2	

III.SIMULATION AND MEASUREMENT RESULTS

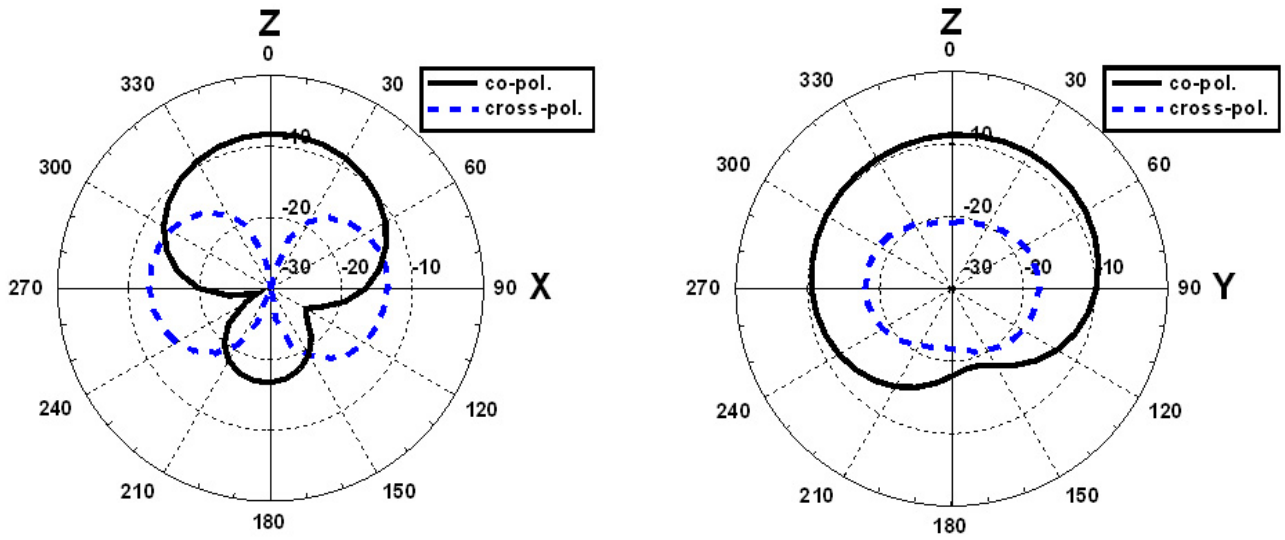

Fig.4 Simulated antenna radiation power patterns in the XZ-plane and YZ-plane at 60GHz.

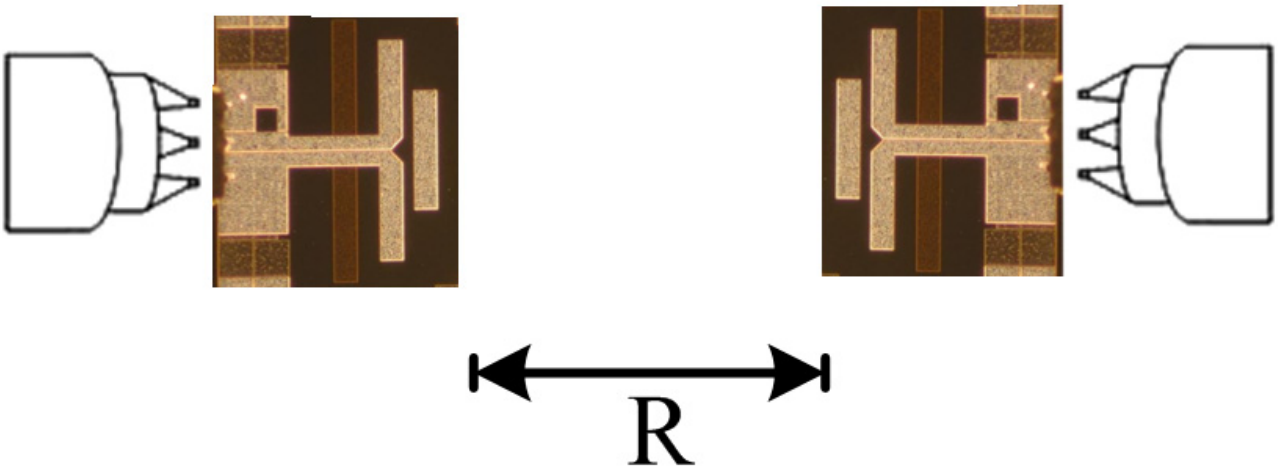

Fig.5 Illustration of the on-wafer measurement setup for the power gain of the on-chip antenna.

Fig.3 shows the fabricated CMOS Yagi-antenna chip micrograph and on-wafer measured input VSWR. The chip size is 1.1 x 0.95 mm^2. The input VSWR of the CMOS antenna is less than 2 from 55 to 65 GHz. Fig. 4 shows the simulated antenna radiation power patterns in the XZ-plane and YZ-plane at 60GHz. The simulated maximum antenna power gain and the front-to-back ratio at 60GHz are about -8 and 9 dB, respectively. Note that the antenna power gain (absolute gain) Gp is defined as

G_p = directive gain × radiation efficiency. (1)

The simulated antenna radiation efficiency is about 10 %, which may be due to the CMOS substrate loss. The absolute power gain of the antenna was measured on-wafer with the technique presented in [13]. In the on-wafer antenna power gain measurement, two identical on-chip antennas are placed face-to-face with a distance R, as shown in Fig. 5. One antenna is used as a transmitting antenna and the other as a receiving antenna. It is noted that the separated distance R between two identical antennas should be satisfied with the far-field condition, which is equal to or greater than $R = 2D^2/\lambda_0$ [13], where D and λ_0 are the largest aperture dimension of the on-chip antenna and the free-space wavelength at the operating frequency, respectively. From the Friis power transmission formula, the maximum antenna power gain (in the central forward direction of the antenna) is given by

$$G_r G_t = G^2 = \left(\frac{P_r}{P_t}\right)\left(\frac{4\pi R}{\lambda_0}\right)^2 = |S_{21}|^2\left(\frac{4\pi R}{\lambda_0}\right)^2 \qquad (2)$$

where G_t and G_r is the power gain of the transmitting and receiving antenna, P_t is the power transmitted, and P_r is the power received. Similarly, since the two antennas are identical, $G_t = G_r = G$. The power ratio P_r / P_t is the measured direct transmission coefficient $|S_{21}|^2$ from the vector network analyzer (VNA). The measured maximum antenna power gain at 60 GHz is about -10.6 dBi. Table I shows the performance summary of the antenna radiation characteristics. Table II lists the performance comparison of the 60-GHz CMOS on-chip antenna with the reported work.

TABLE II PERFORMANCE COMPARISON WITH REPORTED WROKS

	CMOS Process	Freq (GHz)	VSWR	Power Gain (dBi)	F/B ratio (dB)	Chip Size (mm^2)	Efficiency(%) (Simu.)
[3] (Qusi-Yagi)	post-back-end-of-line (post-BEOL)	61-70	< 3 (RL< 6 dB)	-12.5 @ 65-GHz	**poor**	~1.1*	5.6
This work (Yagi)	Standard 0.18 μm	55-65	< 2	-10.6 @ 60-GHz	9	1.05	10

*Axial length = 1.3 mm

IV.CONCLUSION

A 60-GHz millimeter-wave on-chip Yagi antenna is presented for 60-GHz WPAN CMOS transceiver application. The CMOS antenna is fabricated with a 0.18-μm standard CMOS process. The antenna chip size is 1.1 × 0.95 mm^2. A feeding network is designed in coplanar waveguide technology. Compare with the qusi-Yagi antenna, the 0.18 μm 6-metal-layer CMOS process allows the proposed Yagi antenna to utilize the first metal-layer (M1) to implement a reflector strip. The on-wafer measurement is conducted to measure the input SWR and the maximum antenna power gain of the on-chip antenna. The simulated antenna radiation efficiency is about 10 %, which may be due to the CMOS substrate loss. The simulated antenna pattern performs an end-fire radiation characteristic, and the front-to-back ration is about 9 dB. The measured input VSWR less than 2 from 55 to 65 GHz. The maximum antenna power gain at 60 GHz is about -10.6 dBi. The designed on-chip Yagi antenna is useful for the integrated design of the 60-GHz CMOS single-chip RF transceiver.

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