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Characteristics of an InP/InGaAs Double Heterojunction Bipolar Transistor (DHBT) with an InAlGaAs/InP Composite Collector Structure

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In recent years, heterojunction bipolar transistors (HBTs) have attracted great attention for high-speed, low-power and microwave circuits applications. Nevertheless, based on the high impact ionization rate in the narrow bandgap InGaAs base layer, these conventional HBTs with the InGaAs collector structure are strongly limited for their power applications due to the low breakdown voltage and the high output conductance. Although the improved breakdown performance can be achieved by using a wide bandgap InP layer as the collector in double HBTs (DHBTs), the conduction band discontinuity at the base-collector (B-C) interface should lead to the undesired current blocking effect. To overcome such disadvantages, several attempts have been made and reported to fabricate high-performance HBTs. These improved structures include the composite collector structure and the compositionally graded layer. Previously, an InGaAs/InAlAs chirped superlattice (CSL) of InP/InGaAs DHBTs with a continuous InAlGaAs grade layer was demonstrated to produce the InP/InGaAs DHBTs. On the other hand, a step-graded InGaAsP collector structure in an InP/InGaAs DHBT was also reported.

In this work, an interesting InP/InGaAs DHBT with an InAlGaAs/InP composite collector structure is fabricated and studied. In this structure, the composite collector consists of an InGaAs setback layer, a step-graded structure, and an InP layer. Moreover, the step-graded structure uses a quaternary InAlGaAs material between base and collector layer. The InAlGaAs material system has a wider tunable bandgap (0.75 to 1.46 eV) than the InGaAsP material system (0.75 to 1.35 eV). Due to the use an InAlGaAs/InP composite collector structure, the undesired current blocking effect can be effectively eliminated. Furthermore, the breakdown characteristics can be improved.

The collector-emitter offset voltage ΔV_{CE} as a function of the temperature is shown in the Fig. 1(a). The offset voltageΔV_{CE} is defined as the collector-emitter voltage at which the collector current reaches zero. Under the base current of I_B = 20μA, the offset voltageΔV_{CE} is slightly increased from 98.4 to 100.98 mV as the temperature is elevated from 300 to 450 K. The studied device shows relatively lower offset voltage even the temperature is increased up to 450K. The smaller offset voltage is attractive in practical circuit applications due to the lower power consumption. On the other hand, the output resistance, which can be characterized by the Early voltage V_A, is an important issue for transistor action. The V_A as a function of temperature of the studied device is shown in Fig. 1 (b). The base current is kept at I_B = 100μA. Actually, the operating region of InGaAs-based devices is adversely determined by the onset of impact ionization. In particular, at higher temperature ambient, the increase of output conductance and decrease of breakdown voltage result in the reduction of current operating region. The V_A value of the studied device is remarkably superior at least 4 times in magnitude to those observed from InP/InGaAs HBTs with InGaAs collector or InGaAs/InGaAsP composite collector. This is mainly attributed to the lower multiplication factor M-1 values resulted from the relatively higher effective energy bandgap of the studied device with the InAlGaAs/InP composite collector structure.

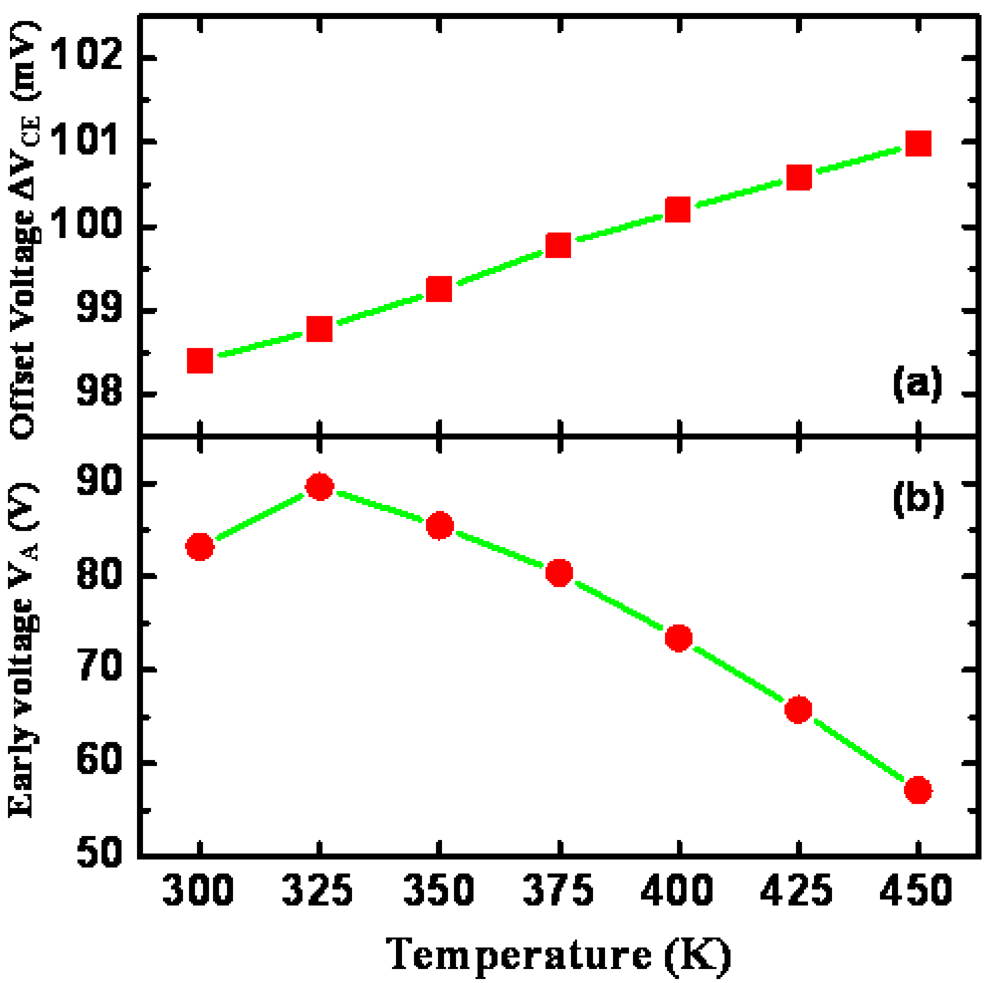

Fig. 1 (a) The collector-emitter offset voltageΔV_{CE} as a function of temperature. (b) The temperature dependences of Early voltage V_A.

Figure 2 shows collector leakage current I_{CBO} as a function of temperature under different reverse collector-base voltage V_{CB}. Generally, the I_{CBO} is substantially related to the B-C layer structure. From the experiment result, a positive temperature dependence of I_{CBO} is found. Under the lower reverse bias region ($V_{CB} < 6$ V), the I_{CBO} values are smaller than those observed in InP/InGaAs HBTs with an InGaAs collector and an InAlGaAs collector. Under the higher reverse bias region ($V_{CB} > 6$ V), a strong bias-dependent phenomenon is found owing to the avalanche effect. Therefore, the I_{CBO} is significantly increased. As the temperature is increased, the impact ionization phenomenon becomes important and leads to the rapid increase of the I_{CBO}. Furthermore, the raised I_{CBO} causes the substantial avalanche multiplication, which certainly results in the decreases of breakdown voltage.

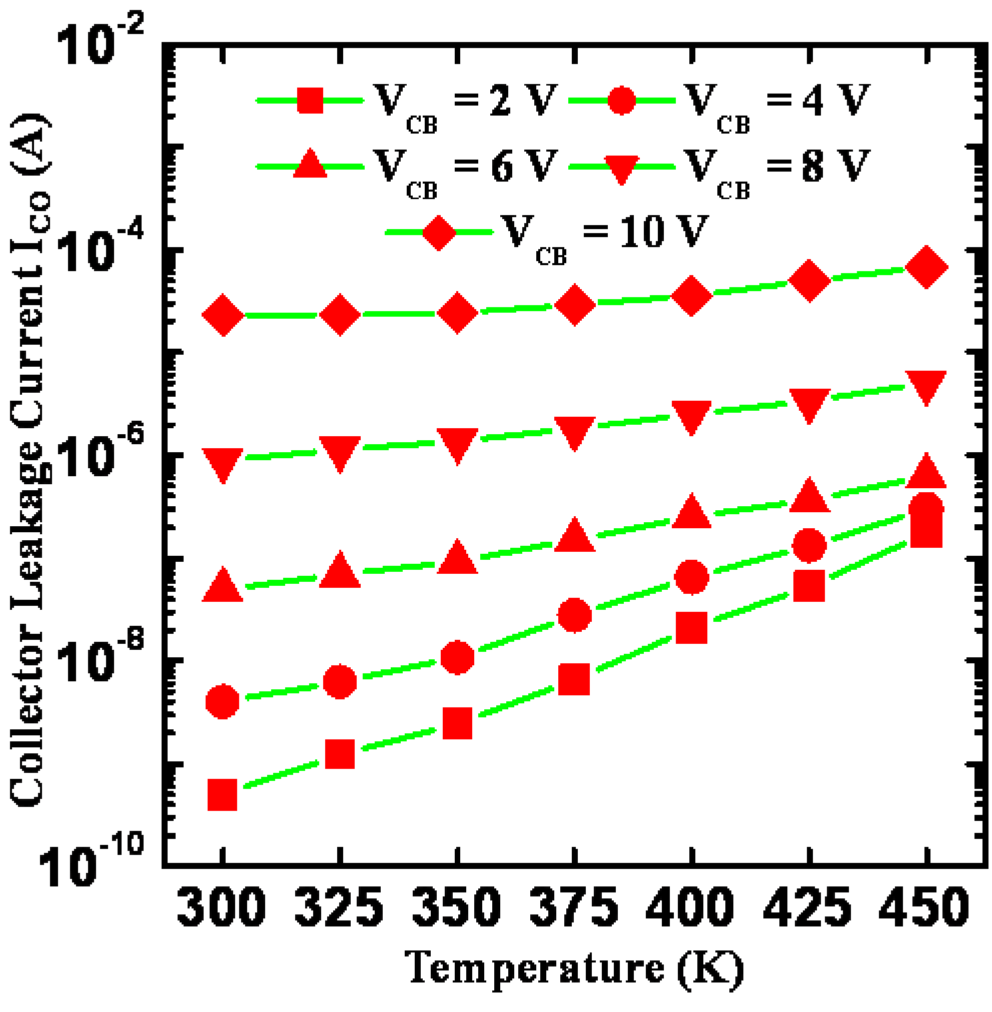

Fig. 2 Collector leakage current as a function of temperature under different collector-base voltage V_{CB}.

Figure 3 displays the multiplication factor M-1 as a function of collector-base voltage V_{CB} at different temperatures for the studied device. For comparison, other results of the previously reported InP/InGaAs HBT with an InGaAs collector are also demonstrated. As shown in Fig. 3, the M-1 values are increased with increasing both the V_{CB} and temperature. For V_{CB} ranged from 2 to 8 V, the M-1 values for our studied device are about one to two orders of magnitude lower than those obtained in the InP/ InGaAs HBT with an InGaAs collector. It reveals the substantial suppression of the avalanche effect in the B-C depletion region due to the use of an InAlGaAs/InP composite collector structure. The lower M-1 values of our device are caused by the effective higher energy bandgap of the InAlGaAs/InP composite collector structure with a thicker InP layer. Therefore, the M-1 values in our collector structure are mainly dominated by the InP layer. Based on the relatively thicker InP layer in our collector structure, as compared with the InP/InGaAs HBT with an InGaAs collector, the studied device exhibits improved breakdown performance resulting from the lower M-1 values.

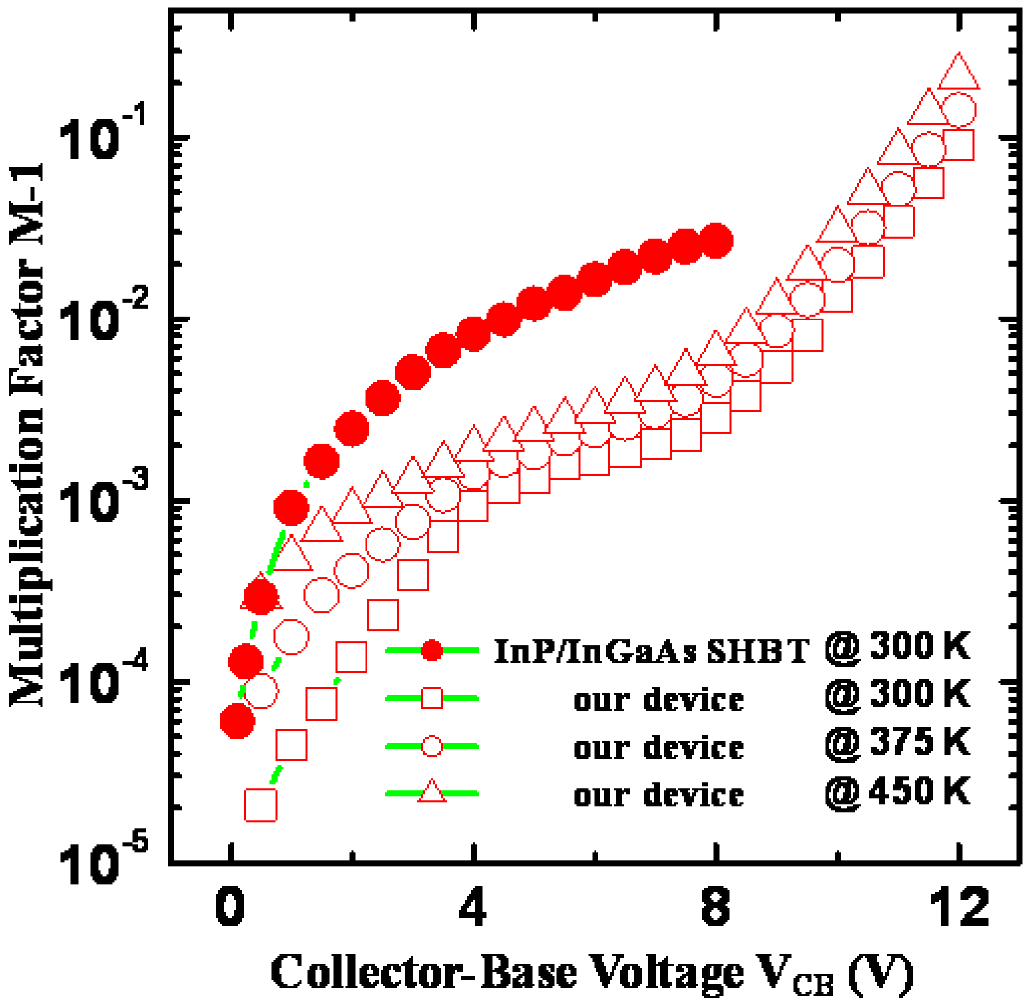

Fig. 3 The multiplication factors M-1 versus collector-base voltage V_{CB} at different temperatures for the studied device and compared InP/InGaAs SHBT.

The DC current gain variation $\Delta\beta_F$ (%), under I_C = 10 mA, versus the stress time of the studied device at the ambient temperature of 450 K is revealed in Fig. 4. The applied collector-emitter voltage is kept at V_{CE} = 3 V. After a 180 hr of stress test, the β_F of our studied device drops 6.89 % from its initial value. Experimentally, it is found that the bias stress could cause an increase of the base current, which certainly results in the decrease of the β_F. Clearly, the studied device exhibits lower$\Delta\beta_F$ during the life test. The hot carrier-induced damage localized at E–B and B–C junction peripheries could be responsible for the increase of B–C junction leakage and decrease of current gain during bias stress. Therefore, from Fig. 4, the studied device with an InAlGaAs/InP composite collector structure exhibits the improved thermal stability and electrical reliability.

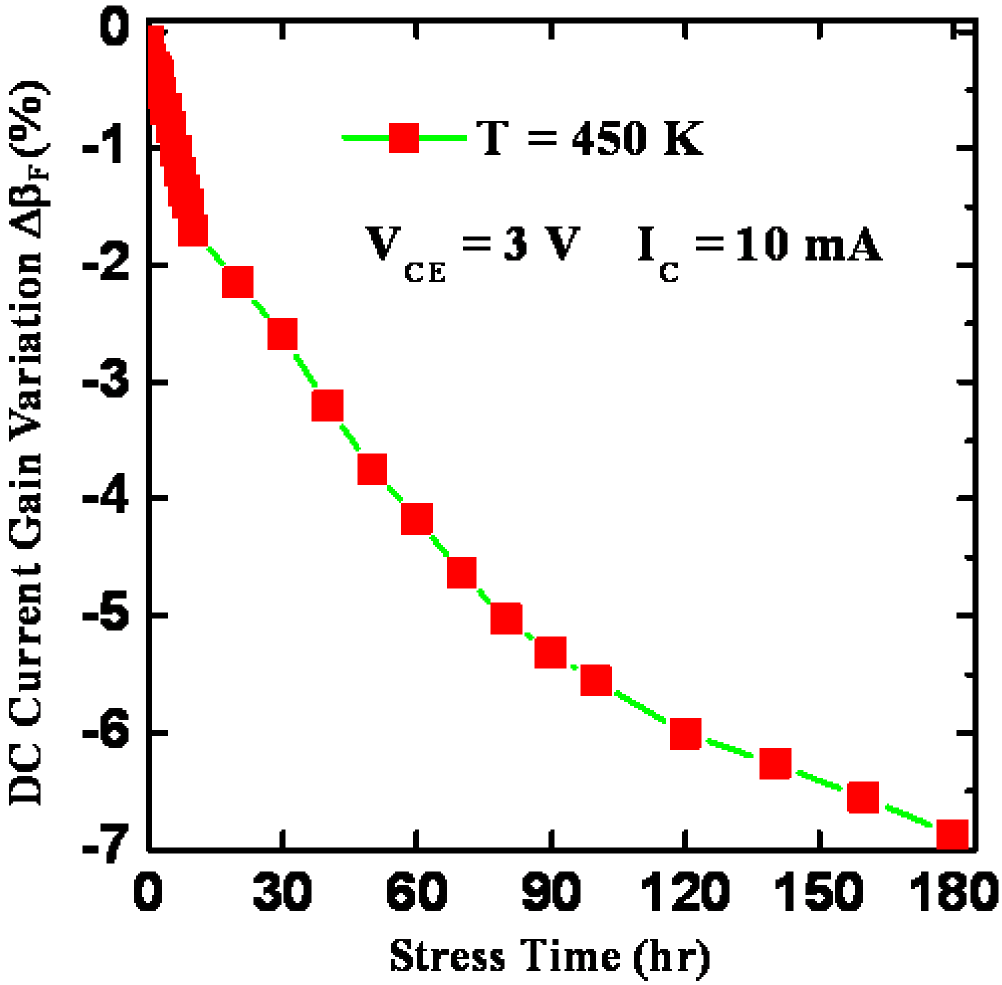

Fig. 4 The DC current gain variation $\Delta\beta_F$ (%) versus the stress time. The stress conditions are kept at V_{CE} = 3 V and I_C = 10 mA.

In conclusion, the characteristics of an interesting InP/InGaAs DHBT with an InAlGaAs/InP composite collector structure are demonstrated and studied. Experimentally, as compared with previously reported HBTs, the studied device exhibits the relatively larger Early voltage, lower offset voltage, smaller collector leakage current, and lower multiplication factor. Furthermore, the electrical reliability for studied device is also reported. Therefore, the studied DHBT device provides the promise for power and high-temperature circuit applications.