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Off-State Avalanche Breakdown Induced On-Resistance Degradation in Lateral DMOS Transistors

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Recently, lateral DMOS (LDMOS) transistors are widely used in medium-voltage smart-power applications because they are easily integrated into the mature standard CMOS process. When the LDMOS device is used in switching applications, the device experiences avalanche breakdown during on-state to off-state transient because of unclamped inductive load. The maximum electric field of the LDMOS device in avalanche occurs at the Si/SiO_2 interface near the drain side. Even if a rugged device survives breakdown initially, repeatedly operating under avalanche may gradually wear out the device because of high electric field near the drain. To evaluate this reliability concern, this work presents the on-resistance (R_{on}) degradation of LDMOS transistors caused by avalanche breakdown.

Devices investigated in this study are n-type LDMOS transistors fabricated by a 0.35 μm CMOS compatible technology. The cross section of the device, potential contour, impact ionization contour, and electric field distribution biased under avalanche breakdown is shown in Fig. 1. The channel region (Lch) and accumulation region (Lacc) are also indicated in the figure. The device has the following characteristics: the typical operating drain voltage (V_{ds}) and gate voltage (V_{gs}) is 12 V, off-state breakdown voltage is 19.3 V, and R_{on} is 7 $m\Omega\text{-}mm^2$. To evaluate the damage created during fast on-off transient, constant-current pulse stressing is applied to the drain and grounding the source, gate, and p-channel terminals. The stressing is performed at room temperature with various current levels ranging from 1μa to 1 mA. The duration of each pulse is 0.1 s and the number of pulses is 100. During the stressing, R_{on} is monitored periodically. In addition, charge pumping current (I_{CP}) is measured to extract stress-induced interface state density (ΔN_{it}) and oxide trap density (ΔN_{ot}). The pulse in charge pumping measurement is applied to the gate while the drain and p-channel terminals are grounded. The source terminal is floating because the damage near the source side is negligible. The amplitude of the pulse is fixed at 10 V and the base voltage (V_{base}) sweeps from -8 V to 0 V under a frequency of 500 kHz. Process (TSUPREM4) and device (Medici) simulations are also performed to investigate the degradation mechanism under avalanche breakdown condition.

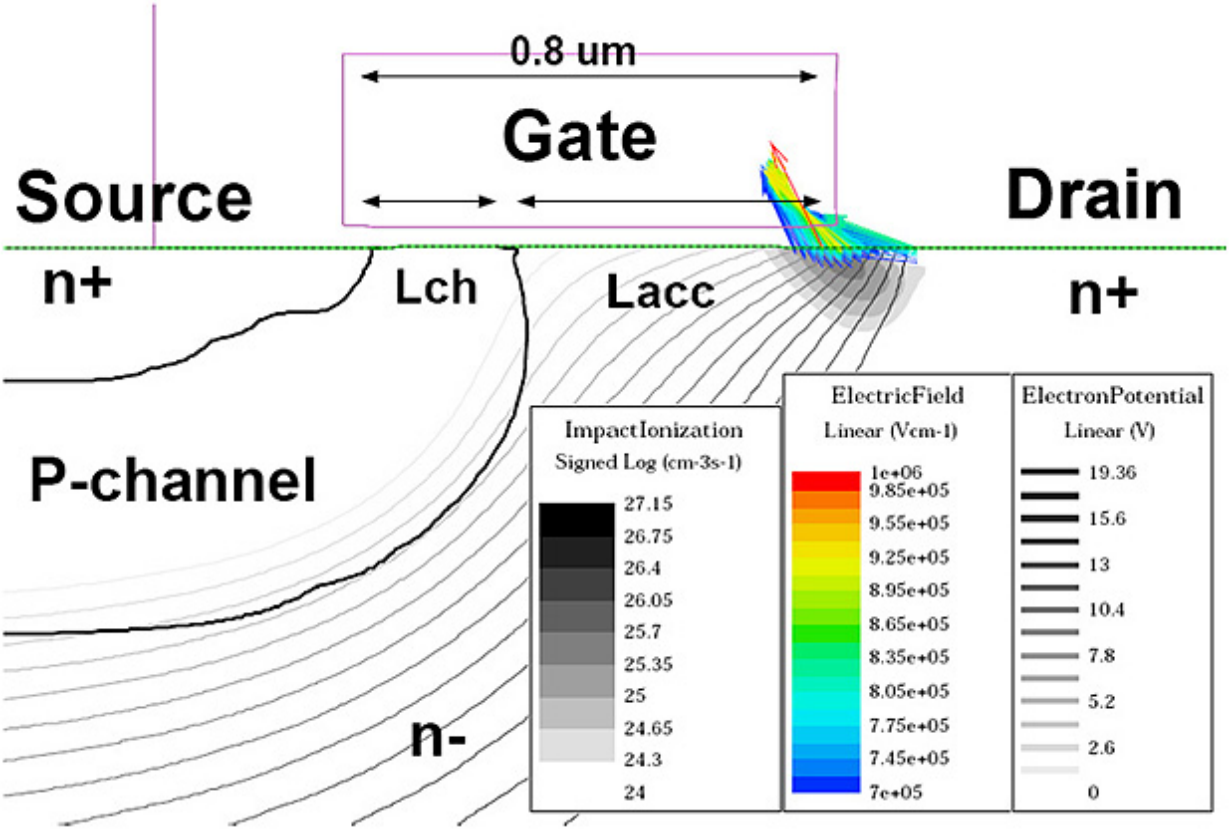

Fig. 1. The device cross section and TCAD simulation results on potential contour (line), impact ionization contour (field), and electric field (vector) of our LDMOS device under avalanche breakdown condition.

The relationship between R_{on} degradation and the number of current pulse under various current levels is shown in Fig. 2 and two observations are found. First, higher current level produces larger R_{on} degradation at the beginning but eventually R_{on} degradation saturates at roughly 14%. Second, the magnitude of R_{on} degradation is closely related to the product of current level and the number of pulses. For instance, the R_{on} degradation under 10•• stressing for 10 pulses is roughly equal to the R_{on} degradation under 100•• stressing for 1 pulse. Such a result reveals that avalanche-breakdown-induced damage is determined by the total charge flowing through the drain. To identify the mechanism of breakdown-induced R_{on} degradation, charge pumping measurement and TCAD simulation are performed. Fig. 3 shows the I_{CP} data of the device before and after 10μa current pulse stressing. Based on TCAD simulation results of flat-band voltage and threshold voltage along Si/SiO_2 interface, it can be found that ΔN_{it} located in the Lch, Lacc, and spacer region can be sensed when V_{base} = -8 V. At V_{base} = -4 V, however, only ΔN_{it} created in the Lch and Lacc region can be probed. According to I_{CP} data in Fig. 3, little increase of I_{CP} (ΔI_{CP}) at V_{base} = -4 V but significant ΔI_{CP} at V_{base} = -8 V indicates that most of the ΔN_{it} appears under the spacer region. To confirm the location of ΔN_{it}, lateral distribution of ΔN_{it} is extracted from ΔI_{CP} data and the result is depicted in the inset of Fig. 3. It shows that ΔN_{it} is distributed under the spacer region centered at 70 nm away from the poly-gate edge and the width of distribution is less than 20 nm.

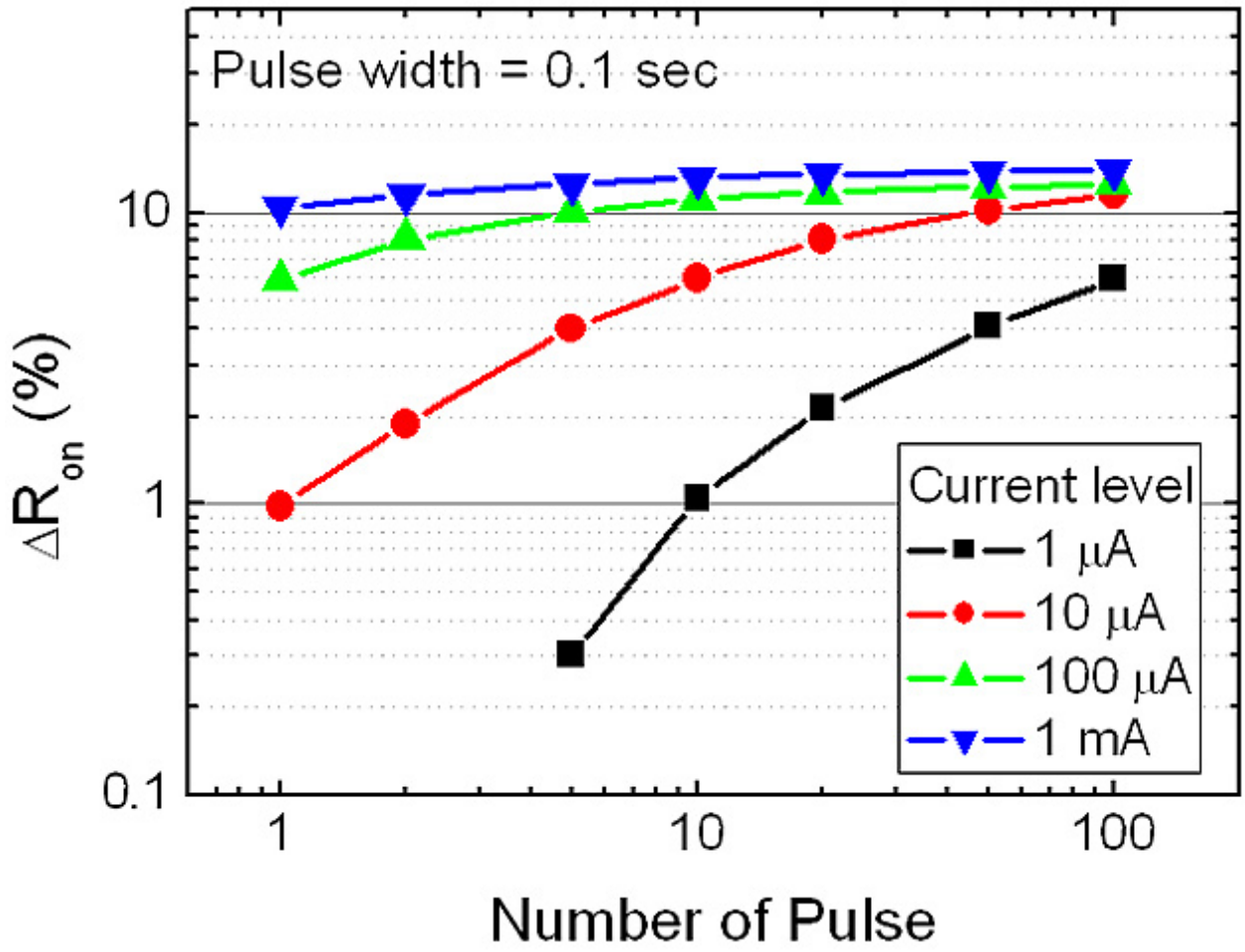

Fig. 2. R_{on} degradation as a function of the number of current pulse under various current levels.

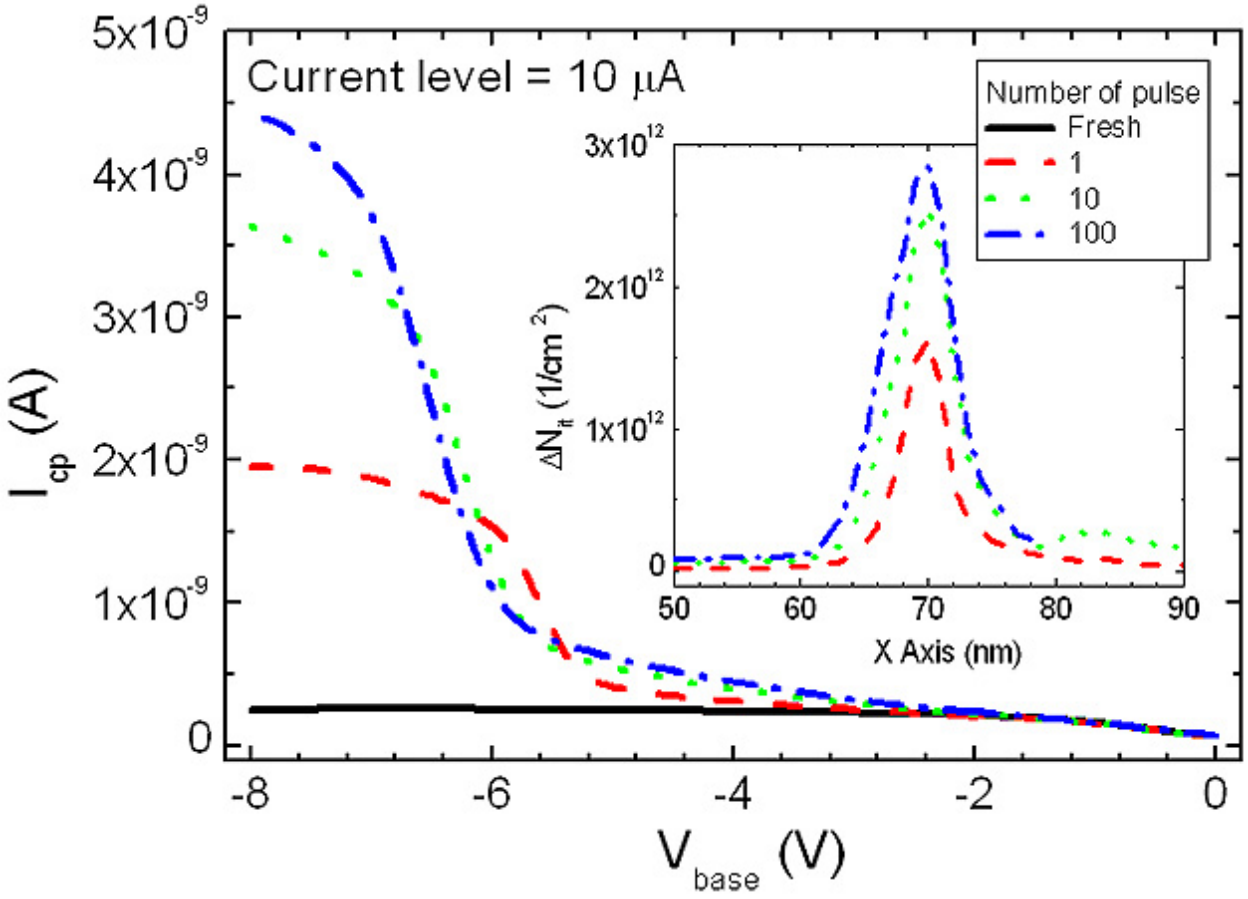

Fig. 3. I_{CP} data of the device before and after 10μa current stressing for 100 pulses. ΔN_{it} distribution is shown in the inset. The origin of X-axis in the inset is the poly-gate edge.

As the number of stress pulse increases, in addition to ΔN_{it}, a left shift in the I_{CP} vs. V_{base} characteristics indicates that positive oxide-trapped charges (ΔN_{ot}) are also created. The density of oxide-trapped charges can be extracted and the peak value of ΔN_{it} distribution and ΔN_{ot} distribution as a function of the number of current pulse is drawn in Fig. 4 and two phenomena are evident. First, ΔN_{it} is roughly 10 times greater than ΔN_{ot}, suggesting that the main mechanism responsible for R_{on} degradation is interface state generation. Second, both ΔN_{it} and ΔN_{ot} saturate as the number of current pulse increases. This trend is identical to the saturation of R_{on} degradation as seen in Fig. 2. The results in Figs. 1 – 4 suggest the mechanisms responsible for breakdown-induced R_{on} degradation are as follows. Avalanche breakdown results in significant impact ionization near the drain. The electrons generated by impact ionization flow to the drain. Most of the holes created by impact ionization go to p-channel. However, some of the holes can inject into the gate oxide because the direction of the electric field near the drain is from drain toward the gate as in Fig. 1. Such hole injection leads to interface state generation and positive oxide-trapped charges. Although positive ΔN_{ot} can attract electrons under the spacer and reduce series resistance, ΔN_{it} is much greater and leading to R_{on} degradation. Since ΔN_{it} is distributed in a narrow region, the available interface trap sites are limited, leading to the saturation of ΔN_{it}. Positive ΔN_{ot} also has the tendency to saturate as in Fig. 4. The saturation of ΔN_{it} and ΔN_{ot} is responsible for the saturation of breakdown-induced R_{on} degradation.

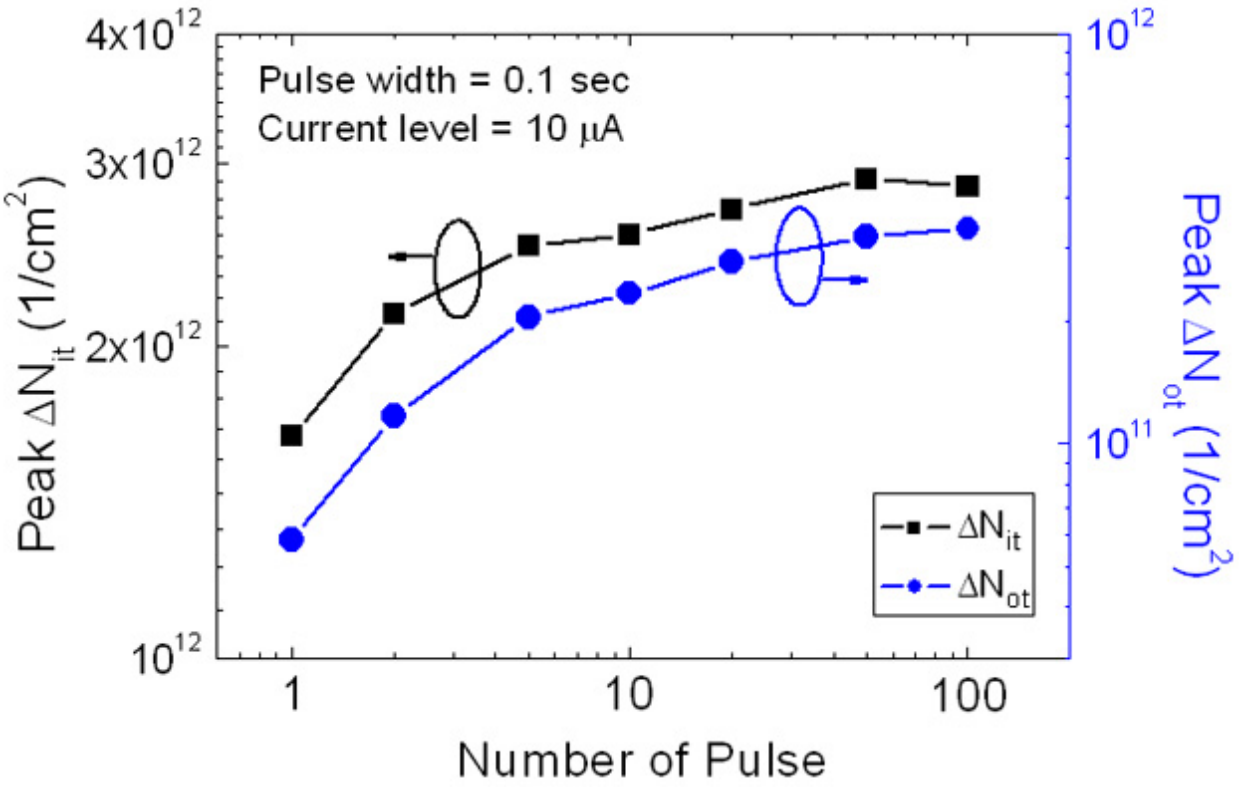

Fig. 4. The peak value of ΔN_{it} and ΔN_{ot} as a function of the number of current pulse.

In conclusion, R_{on} degradation in LDMOS transistors operated under avalanche breakdown has been discussed. Interface state generation is the main degradation mechanism. TCAD simulation suggests that the driving force of damage is breakdown-induced hole injection near the drain. The degradation of R_{on} saturates because of the saturation in interface state generation. Since the device experiences avalanche breakdown during unclamped inductive switching, breakdown-induced R_{on} degradation should be taken into consideration during product design and manufacturing.