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# High-Temperature Stable HfLaON p-MOSFETs With High-Work-Function $Ir_3Si$ Gate

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Based on the International Technology Roadmap for Semiconductors, the metal-gate/high-κ is the required technology for the future generation complementary MOSFETs to reduce the undesired large gate leakage current and continue the gate oxide scaling. Metal gate electrode is also essential to overcome conventional poly-Si gate problems such poly depletion, boron penetration and high resistivity. Currently, the HfSiON is a promising candidate beyond SiON with merits of high-κ value, low gate leakage current, and similar amorphous structure after 1000℃rapid thermal annealing (RTA) for self-aligned process. However, the lack of a high work function gate for HfSiON p-MOSFETs is the challenge since only Ir (5.27 eV) and Pt ( 5.65 eV) in the periodic table have the needed work function larger than the target 5.2 eV. The other problem of HfSiON is the relative lower κ of 10~14 that causes limited scaling capability. We developed the high temperature stable $Ir_3Si$/HfLaON p-MOSFET to address the aforementioned issues. The novel HfLaON dielectric can preserve the amorphous structure after 1000℃RTA and is similar to HfSiON but with significantly higher κ value. Using high work-function $Ir_3Si$ gate electrode, the p-MOSFETs show good device integrity of low leakage current of $1.8 \times 10^{-5}$ A/cm$^2$ at 1 V above flat-band voltage $V_{fb}$, high effective work function $\phi_{m\text{-}eff}$ of 5.08 eV, high hole mobility of 84 cm$^2$/V-s, and good 1000℃ RTA thermal stability at equivalent oxide thickness (EOT) of 1.6 nm. These results are compatible with or better than the best reported metal gate high-κ p-MOSFETs.

In the experiment, standard N-type Si wafers with resistivity of 1–10 Ω-cm ($10^{15}$~$10^{16}$ cm$^{-3}$ doping level) were used in this study. After standard RCA clean, the HfLaO was deposited on N-type Si wafers by physical vapor deposition and post-deposition annealing. The HfLaON was formed by applying NH3 plasma surface nitridation on HfLaO. Then 5 nm amorphous-Si and 20 nm Ir were subsequently deposited on HfLaON and RTA annealed at 400~1000℃ for 30~5 sec to form the MOS capacitors. For comparison, Ir/HfSiON devices were also fabricated, where the HfSiON was formed by atomic layer deposition of HfSiO and followed by surface plasma nitridation.

The low-temperature-deposited Al gate on 1000℃RTA-annealed HfLaON capacitors was also formed for $\phi_{m\text{-}eff}$ reference. For p-MOSFETs, additional thick TaN capping layer is added on Ir/Si/HfLaON to prevent subsequent ion implantation penetration, where the IrxSi gate was formed during RTA. After patterning, self-aligned $B^+$ implantation was applied at 25 keV, and source/drain doping was activated at 1000℃ RTA for 5 sec. The fabricated p-MOSFETs were characterized by capacitance–voltage (*C*–*V*) and current–voltage (*I*–*V*) measurements.

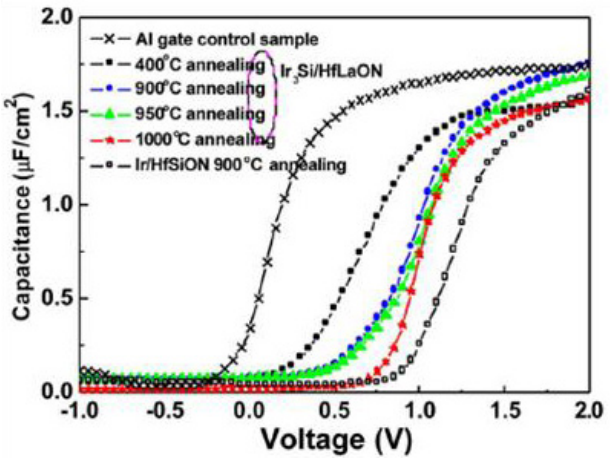



Fig. 1. (a)*C*–*V* characteristics of $Ir_xSi$/HfLaON, Ir/HfSiON, and Al/1000℃-annealed HfLaON capacitors

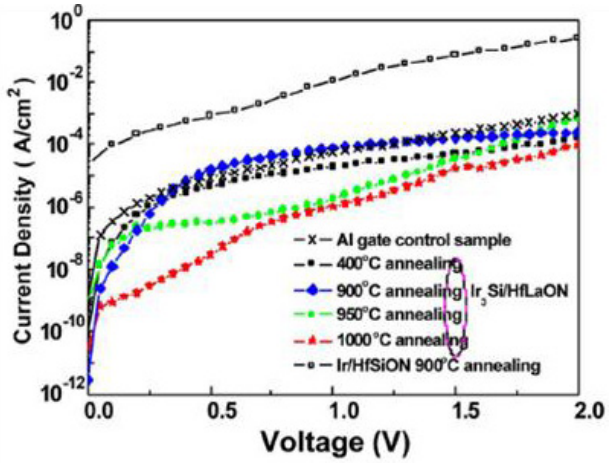
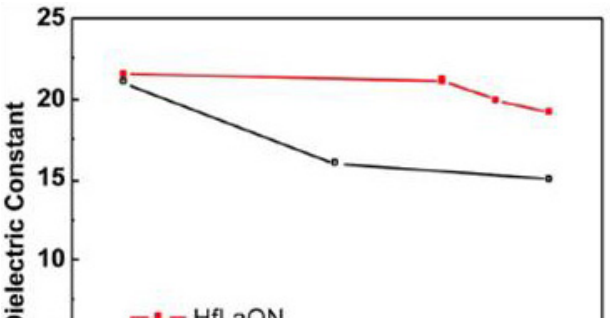
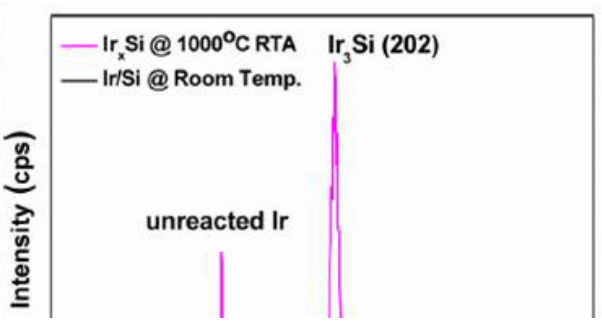



Fig. 1 (b)*J*–*V* characteristics of $Ir_xSi$/HfLaON, Ir/HfSiON, and Al/1000℃-annealed HfLaON capacitors

Figure 1(a) and (b) shows the *C*–*V* and *J*–*V* characteristics, respectively, for different RTA temperature-annealed IrxSi/HfLaON capacitors. The Ir/HfSiON and Al/1000℃annealed HfLaON devices are also shown for comparison. An increasing $V_{fb}$ trend with increasing RTA temperature is measured, which is attributed to IrxSi reaction toward high-κ interface. The Ir on HfSiON shows the highest $V_{fb}$, but the capacitor failed after 1000℃ RTA. In contrast, the IrxSi/HfLaON has good 1000℃thermal stability by converting Ir to IrxSi by inserting ~5 nm amorphous Si, however, the better thermal stability is traded off the slightly lower $V_{fb}$. From the C–V shift to control Al gate on 1000℃ RTA annealed HfLaON, the extracted $\phi_{m\text{-}eff}$ of $Ir_3Si$/HfLaON is 5.08 eV. Here, the Al-gated capacitor was chosen as a reference because low-temperature-deposited pure metal has little Fermi-level pinning on high-κ dielectric and the same 1000℃ RTA ensures the similar oxide charge in HfLaON to $Ir_3Si$-gated devices. The Al control gate is used to avoid oxide charge difference on thickness introduced by nitrogen-plasma treatment and process variation. Nonetheless, the fixed charge density should be small from the good mobility shown as follows. The merit of using HfLaON rather than HfSiON is clearly seen by the orders of magnitude leakage current improvement. Very low leakage current of $1.8\times10^{-5}$ A/cm$^2$ at 1 V above $V_{fb}$ is measured in IrxSi/HfLaON at 1.6 nm EOT. Such low leakage current is attributed to the high-κ value of 20 and amorphous structure after 1000℃ RTA from cross-sectional transmission electron microscopy measurement. The decreasing stretch of C–V curves with increasing RTA temperature suggests the improving oxide quality, annealing out the defects at high temperatures. Therefore, high $\phi_{m\text{-}eff}$ of 5.08 eV, low gate leakage current of $1.8\times10^{-5}$ A/cm$^2$ ($V_{fb}$ + 1 V), and good thermal stability of 1000℃ RTA can be achieved at the same time in IrxSi/HfLaON MOS capacitors at 1.6 nm EOT. The decreasing capacitance density with increasing RTA temperature is related to slight decreasing κ value reduction shown in Fig. 1(c), but the amount of reduction is significantly less than HfO2.



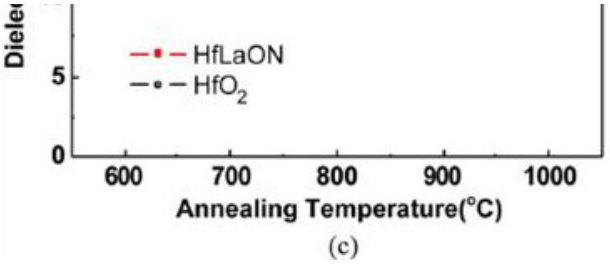



Fig. 1 (c)Dielectric constant of HfLaON and HfO2 at different RTA temperatures

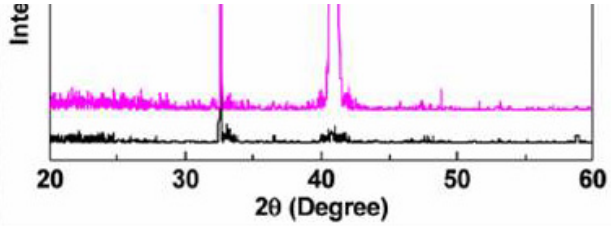



Fig. 2 XRD profiles of the $Ir_3Si$/HfLaON structure

We have further used the X-ray diffraction (XRD) measurements to characterize the IrxSi. As shown in Fig. 2, the Ir-rich IrxSi with x = 3 was formed with distinct 2θ angle to residual Ir peak. The x = 3 in IrxSi was determined by comparing the measured peak XRD pattern with published data. The amorphous structure of HfLaON was also confirmed by glazing angle XRD measurements even after 1000℃ RTA.

Figure 3 shows the transistor *Id–Vd* characteristics as a function of *Vg–Vt* for 1000 ℃ RTA-annealed $Ir_3Si$/HfLaON p-MOSFETs, and good transistor characteristics are obtained. Here, the Vt is –0.1 V as obtained from the linear Id–Vg plot and consistent with the large $\phi_{m\text{-}eff}$ of 5.08 eV from *C–V* curves. Figure 4 shows the hole mobility plot as a function of gate electric field of $Ir_3Si$/HfLaON p-MOSFETs. High hole mobility of 84 and 63 $cm^2$/V-s are obtained at peak value and 1 MV/cm effective field for $Ir_3Si$/HfLaON p-MOSFETs, respectively. This result is comparable with the reported HfSiON p-MOSFET in the literature with advantages of process compatibility to current VLSI line.

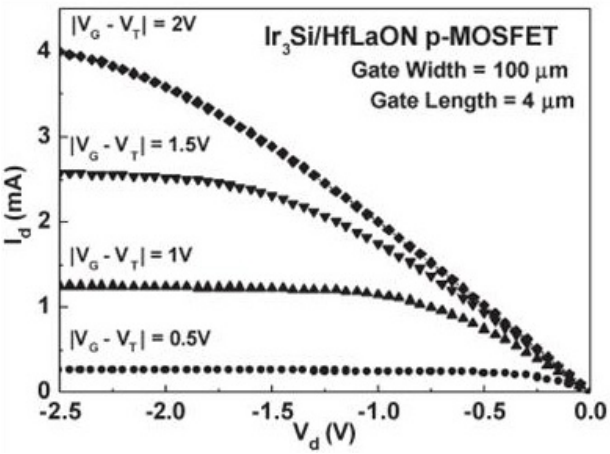



Fig. 3 Id–Vd characteristics of $Ir_3Si$/HfLaON p-MOSFETs. The gate length is 4 μm.

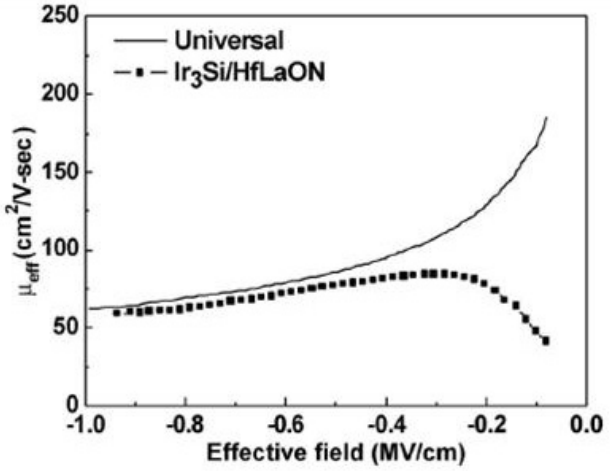



Fig. 4 Hole mobility as a function of gate electric field of $Ir_3Si$/HfLaON p-MOSFETs.

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