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Evaluation of post-annealing-induced defects dynamic behaviors on 90nm In-halo nMOSFETs with low frequency noise and charge pumping measuring techniques

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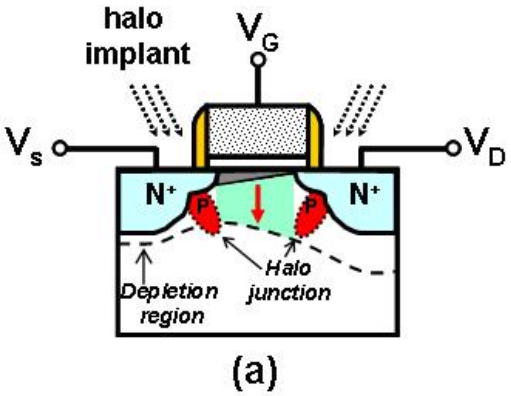
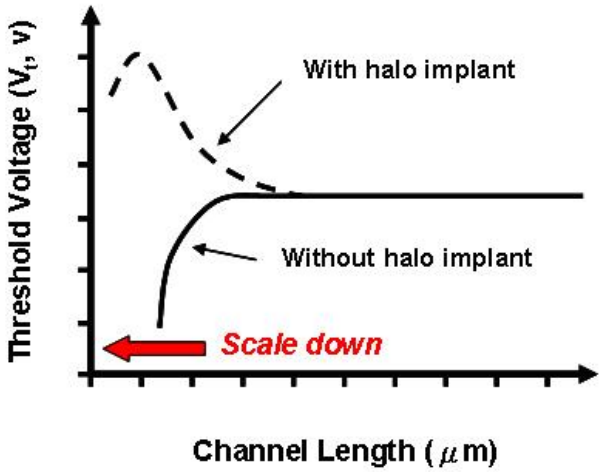
As ULSI (ultra large scale integration) scales down, the threshold voltage shift ΔV_{tL} caused by short channel effect (SCE) becomes serious as shown in Fig.1, especially for nano regime, the ΔV_{tL} grows into a severe issue, thus degrades the device performances significantly. To suppress the SCE, the most popular used technology is halo implantation and followed by a post-thermal annealing (PA). As shown in Fig.2a, the halo implantation is a low energy, low current implantation process with a 45 ° incident angle. The halo implantation reduces the encroachment of S/D on the channel length thus effectively suppressing the SCE, as shown in Fig.2b. Generally, for an nMOSFET both Boron (B) and Indium (In) implantations are used. In nano CMOS technology, the In-halo implantation is preferred for its less diffusion coefficient. However, due to the larger mass of Indium, the In-halo implantation also suffers the higher defects generation, and thus the more degradations of device performances. Hence, needs a post-thermal annealing (PA) after halo implantation.

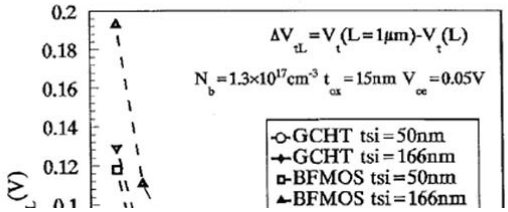


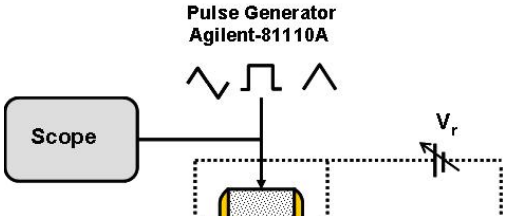
(a)

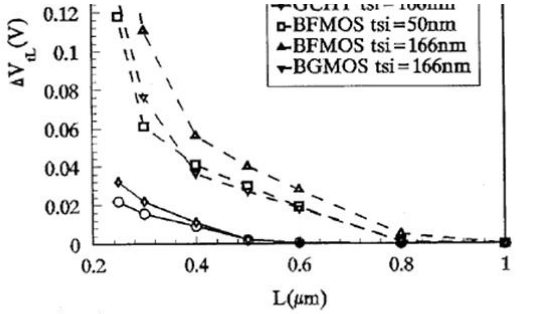


(b)

Fig. 2. (a), Schematic diagram to illustrate a halo implantation process, and (b), comparison of threshold voltage shifts with and without halo implant as a function of the channel length.







資料來源: R. U. Huang and Yang Yuan Wang, "Comprehensive analysis of the short channel effect in the SOI gate controlled hybrid transistor (GCHT)", *INT. J. ELECTRONICS*, Vol. **86**, No. 6, p.685-698, 1999.

Fig. 1. Comparison of threshold voltage shift as a function of the channel length.

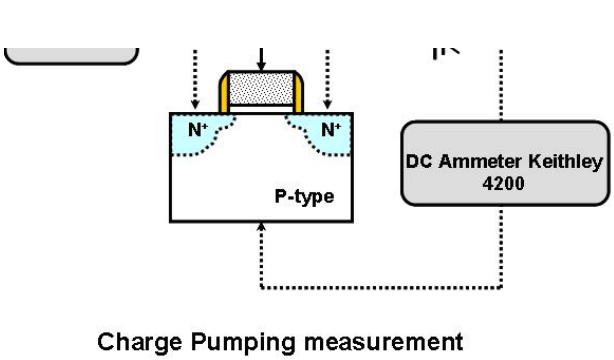


Fig. 3. The schematic diagram of charge- pumping measurement system.

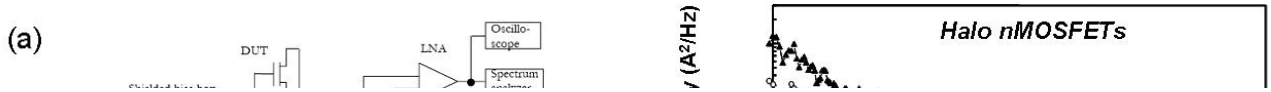
In the past, the In-halo implantation caused degradations and the impacts of various PA processes on the degradations have been studied with conventionally DC analyses. However, they have not investigated the key degradation sources, i.e., gate oxide and Si/SiO_2 interface defects. Besides, the advanced deep-submicron In-halo devices are operated under radio frequency (RF) range; therefore, the DC analysis results are not consistent with the real dynamic operation. Conventionally, with the feature of not affected by the gate leakage, the charge-pumping measurement (CP) becomes most widely used to measure interface state dynamic behavior. This is very important, because in the nano regime the gate leakage is significant due to the thinner gate oxide. Fig.3 illustrates a typical CP measurement diagram, where the source and drain are connected together to a variable bias firstly, and then different frequencies pulses are applied to the gate. As the channel is inversed by the high-level pulse, electrons begin to transport between source and drain, and some of them will captured by the interface states. Which then are recombined with holes in the time of applying low- level pulse, thus contributes the CP current I_{cp} as,

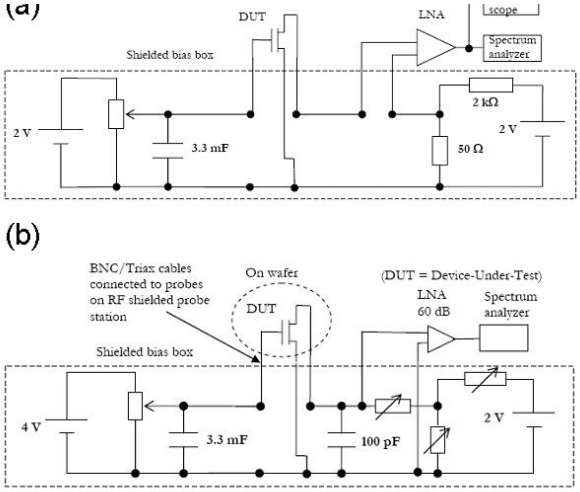
$$I_{cp} = f \cdot Q_{ss} = f \cdot A_G \cdot q^2 \cdot N_{it} \cdot \Delta\psi_s$$

,where f ,A_G, q, N_{it} ,and are pulse frequency, channel area, interface state density ,and surface potential , respectively. Therefore, the N_{it} can be extracted from the measurement of I_{cp}.

Nevertheless, the CP method cannot separate the oxide defects from the interface defects for investigating the PA induced defect dynamic behaviors accurately. Hence, in this work, a high sensitive to both gate oxide and Si/SiO_2 interface defects technology, i.e. the low frequency (LF) noise measurement has been added.

Besides, the LF noise measurement can distinguish the effect of PA on oxide defects from the interface defects. To our knowledge, this is the first report for using LF noise measurement to analyze the defects affected by PA on In-halo. The LF noise measurements were performed on -wafer by using a RF shielded probe station. The weak noise from the device is amplified by a low-noise amplifier and then fed to the signal analyzer, which measures the power spectral density. The output from the amplifier is also monitored by an oscilloscope, which is important in order to detect noise shape and check that the amplifier is not saturated. Two types of amplifiers are frequently used in low frequency noise measurement setups. Fig. 4(a) describes a setup with a low-noise voltage amplifier, which amplifies the voltage at its high impedance input and presents a voltage at the output amplified by a factor A. The setup in Fig. 4(b) is operated with a low-noise current amplifier, which amplifies the current through its low-impedance input and gives a voltage at the output amplified by the trans- impedance gain G.





資料來源: Doctoral Thesis by Martin von Haartman, "Low-frequency noise characterization, evaluation and modeling of advanced Si- and SiGe-based CMOS transistors", *Laboratory of Solid State Devices, School of Information and Communication Technology, Royal Institute of Technology*,2006.

Fig. 4. Two kinds of low frequency noise measurement setups. Where (a) is used for high input impedance, and (b) for use low input impedance.

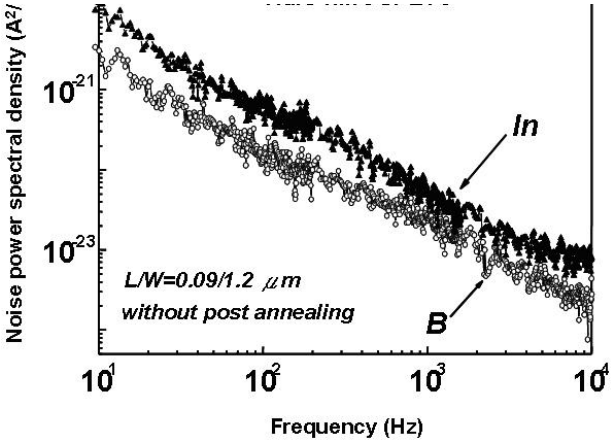
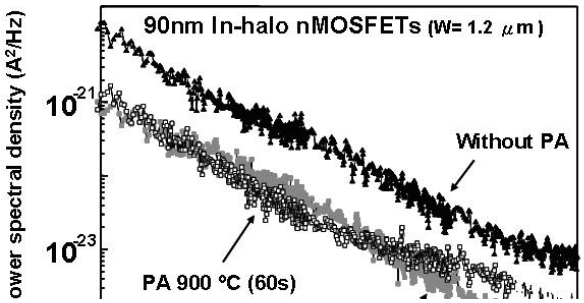
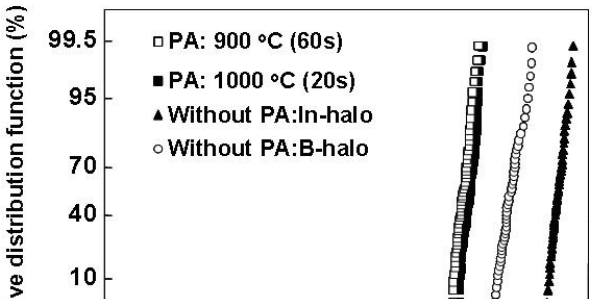


Fig. 5. Noise power spectral density (S_{Id}/Id^2) from 10 Hz to 10 kHz for 90 nm halo-implanted nMOSFETs with no post annealing.

The samples of 90nm In-halo nMOSFET with 1.2 μ m width were prepared by a leading-edge 90nm CMOS technology using shallow trench isolation (STI) and a retrograde well. Fig. 5 shows the measured power spectral density (S_{Id}/Id^2) of 1/f noise from 10Hz to 10 kHz for 90nm B- and In-halo nMOSFETs without PA process, respectively. Devices were measured in subthreshold region under V_D = 0.1V and V_G -V_{TH} = 0.8V. Obviously, without a PA, the noise in In-halo device is higher than that in B-halo one. Moreover, the higher noise in In-halo devices implies that more defects were generated to injure device's DC performances. Various PA treatments were adopted after halo implantation to remove the defects. The noise of In-Halo devices with two different PA treatments was shown in Fig. 6. Apparently, with the 900 ˚ C and long time (60 sec) PA, the noise is lower especially in the region of f <1 kHz. These results are consistent with previous DC work. But for f >1 kHz, the noise in 900 ˚ C long time PA is higher than that with 1000 ˚ C short time PA (20 sec), and contrary to the DC measured results. The results are nicely supported by measuring the gate oxide leakages and charge pumping currents, as shown in Fig.7 and Fig 8, respectively. Fig. 7 gives the cumulative distribution function (CDF) of gate oxide leakages for both the B- and In-halo nMOSFETs. Without the PA treatment, the In-halo devices have a serious gate oxide leakage than that of the B-halo ones .However, after the PA, the gate oxide leakages of all In-implanted samples were greatly reduced and even lower than that of the B-implanted samples especially for the devices with 900 ˚ C long time PA. On the other hand, Fig. 8 shows the differences of the charge pumping currents (I_{CP}) measured in 2M Hz ($ICP_{2\ MHz}$) and 1 MHz ($ICP_{1\ MHz}$). Devices with 900 ˚ C long time PA has higher I_{CP} thus in turn the larger quantity of interface defects.





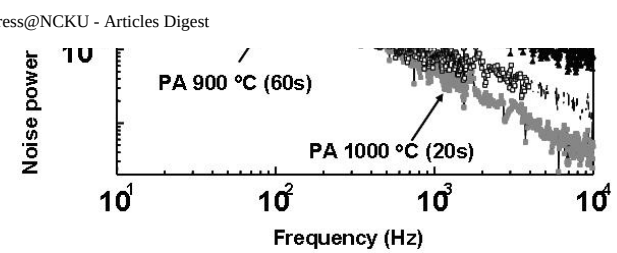


Fig. 6. Noise power spectral density (S_{Id}/Id^2) from 10 Hz to 10 kHz for 90 nm In-halo nMOSFET's under various post annealing treatments.

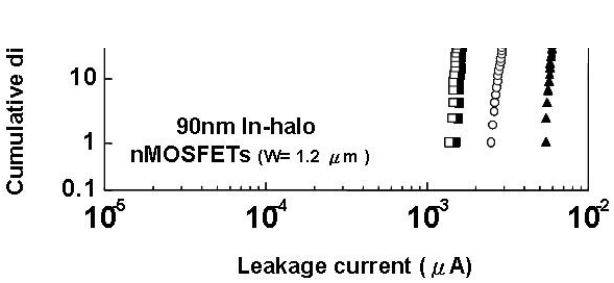


Fig. 7. Gate oxide leakage distributions for nMOSFETs with In- and B-halo structures under various post annealing treatments.

In summary, without PA, low frequency noise measurement in region of f <1 kHz showed that the In-halo implantation increases the noise due to more defects generated in gate oxide and oxide/Si interface. On the other hand, the measurements evidenced the 900 ˚ C long time post-annealing can efficiently mitigate gate oxides defects. However, in region of f >1 kHz, devices with long time PA have higher noise due to more interface defects are generated. Furthermore, the noise in In-halo devices with and without a PA is lower and higher than that in B-halo devices, respectively. Thus, the PA after the In-halo implantation is an indispensable process, but the compromise between the elimination of gate oxide defects and the generation of interface defects should be considered also.

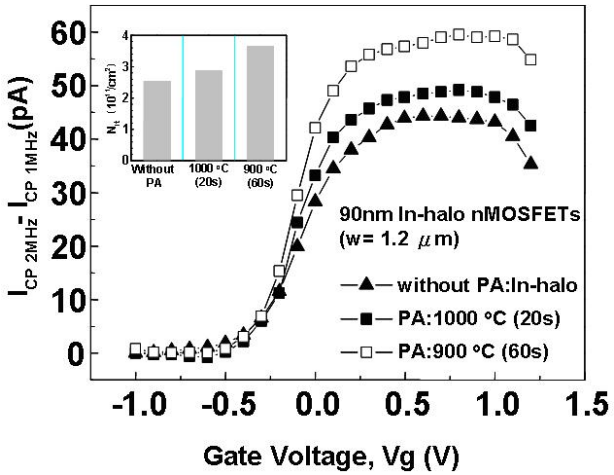


Fig. 8. Charge pumping currents for 90nm In-halo nMOSFETs under various post annealing treatments. The insert shows the N_{it} extracted from the $I_{CP\ MAX}$.