English
Research Express@NCKU Volume 1 Issue 6 - September 28, 2007
[http://research.ncku.edu.tw/re/articles/e/20070928/3.html]

Significantly Enhancing 90 nm Node and Beyond FUSI Gated CMOSFET Performance with A New Strain Method

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IEEE ELECTRON DEVICE LETTERS, 28(2), p. 111-3 (2007)

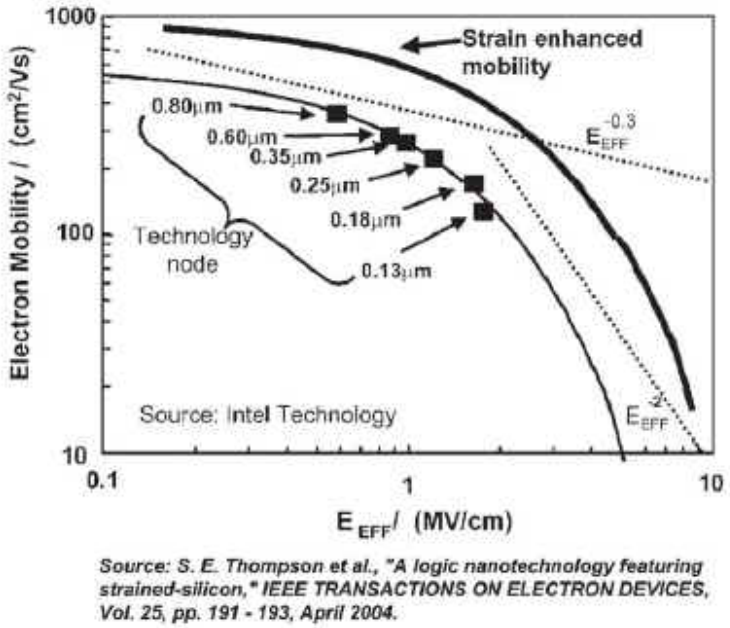
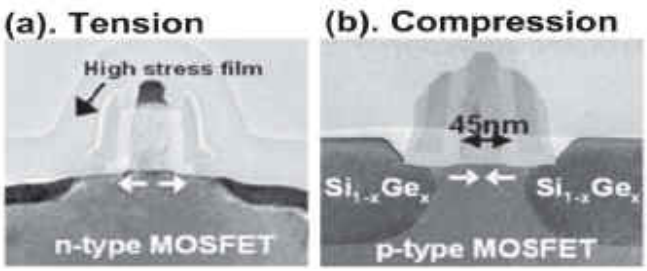


Fig .1 Mobility versus technology scaling trend for Intel process technologies.

To meet the requirement of circuit function expansion, the device density in a ULSI (ultra large-scale integration) chip is increased, thus results in the gate length scaling down. However, a key problem in scaling is the mobility degradation caused by the vertical electric fields, especially as the device scaling to nanoscale; the degradation becomes significant for the field is larger as shown in Fig.1. To counteract this undesirable mobility trend, various higher strain engineering, such as a high-stress CESL (contact etch stop layer) (Fig.2a), selective epitaxial Si1-XGeX in source/drain regions (Fig.2b), to enhance mobility. Usually, the CESL is PECVD(plasma enhanced CVD) deposited high tensile stress SiN, which covers over the gate, and thus give a tensile force to the channel, while the selective epi-Si1-XGeX in S/D offers a compressive force to channel due to the larger lattice constant of Si1-XGeX ((aSi=0.543 nm, aSi1-xGex= x(aGe)+[1-x](aSi), aGe= 0.565 nm) as illustrated in Fig. 3. Then the channel Si is strained by the force. In the strained material, both the conduction band and valence band are spilt, thus enhances the carrier mobility as explained in Fig.4. Besides, various metal gate processes were extensively implemented to replace the conventional poly gate, thus suppressing the poly depletion and improving the device turn on current. Among these metal gates, the FUSI (fully silicided) gate electrode with simple process and tunable work function has become a promising metal gate candidate and been studied widely for future advanced CMOS technology.

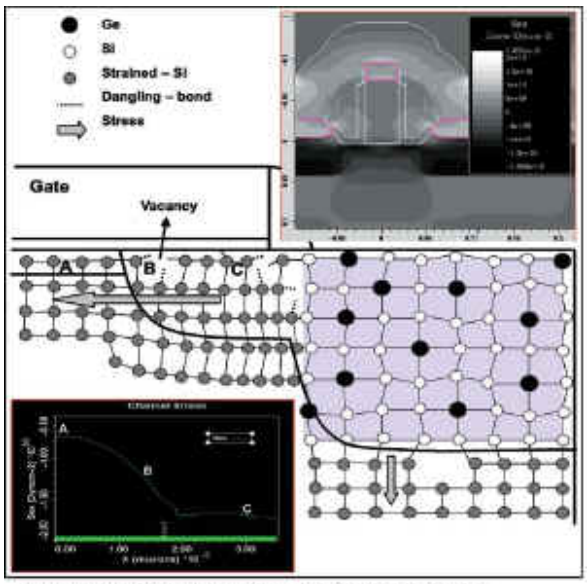
However, in the past, these reported methods are implemented separately and do not meet the requirement well. In this paper, for the first time, we report a new strain engineering method, i.e., integrating the higher



strain engineering with the FUSI metal gate to manipulate higher stress for significantly improved performance. The method involves the use of phase transfer and volume change of a CESL-enveloped FUSI, which is similar to LSC (local strain channel), but can enhance device´s performance more. Most of all, the new method requires neither extra masks nor process steps. It just changes the process sequence of CESL and FUSI RTP2 (the second rapid thermal process of FUSI gate formation). In this work, new strain engineering is demonstrated by the performance enhancement on the CMOSFET with gate length of 60nm by a leading-edge 90-nm CMOS technology. Besides, the simulation confirmation was done with Floops of Synopsys software. The major mechanism of the new strain technique is based on the volume and phase change of the Ni-FUSI gate electrode to give a tensile stress in the channel region by manipulating the composition of Ni-silicide and thermal budget. After FUSI RTP1 (the first rapid thermal process of FUSI gate formation) at 300°C and stripping the non-reacted Ni, a second CESL was deposited to confine NixSi and followed by the RTP2 with different temperatures. The RTP2 resulted in the phase transformation and volume change of Ni-silicide, and thus induced a tensile stress. The curvature difference before and after RTP2 on the blanket wafer was used to measure the stress. Fig. 5 presents the higher tensile stress induced by a higher RTP2 temperature. The results are nicely supported with TEM analysis and XRD spectra. Fig. 6 shows TEM micrographs of the FUSI gate; (a) with RTP2 at 500° C prior to deposition of second CESL, (b) and (c) for the gate with deposition of second CESL firstly then processing

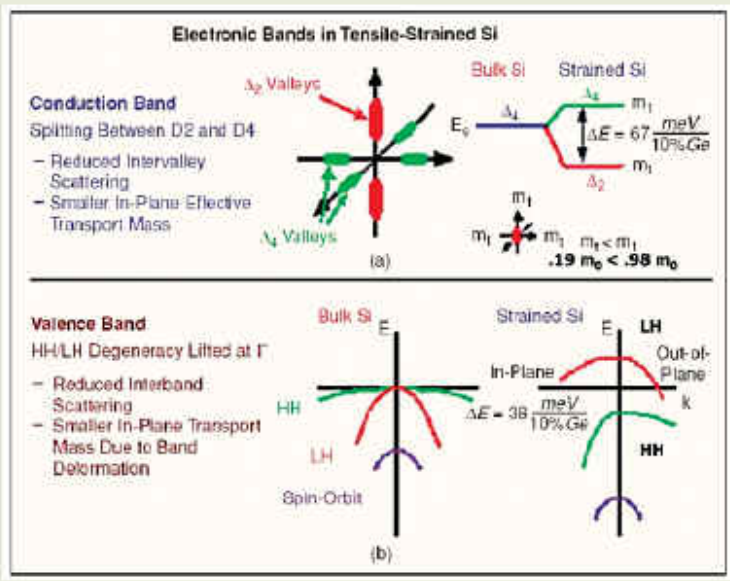
Source: S. E. Thompson et al., "A logic nanotechnology featuring strained-silicon," IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 25, pp. 191 - 193, April 2004.

Fig.2 Various strain technology (a),high-stress CESL, (b), selective epitaxial Si1-XGeX in source/drain regions.



Source: C. Y. Cheng et al., "Investigation and Localization of the SiGe Source/Drain (S/D) Strain-Induced Defects in PMOSFET with 45-nm CMOS Techonology", IEEE Electron Device Lett., Vol. 28, pp. 408 - 411, May 2007.

Fig. 3 The model of embedded SiGe S/D process strain to create a compressive strain. The TSU-PREM IV simulated stress distribution, and the lateral channel stress (Sxx, 5 nm far from the channel surface) are also inserted in the upper, and bottom, respectively.



Source: C.T. Chuang et al.," Scaling planar silicon devices", IEEE circuits and device magazine, Vol. 20, pp. 6-19, Jan-Feb 2004

Fig.4 The spilt conduction band and valence band in the strained silicon.

with RTP2 at 500°C and 700°C,
respectively. Based on the figures, without the envelope of CESL, the step-height of FUSI after 500°C RTP is 30nm, and reduced to 18nm (Fig. 6b) with the enveloped CESL. Simultaneously, the phase of the FUSI is transformed from NixSi (after RTP1 300°C) to NixSiy mixture phase (after RTP2) as is identified by the XRD spectrum on blanket wafer (Fig.7). In addition, based on the confirmation (Fig. 8) by simulation of a narrow gate length device, enveloped FUSI and the reduced step-height generates a tensile stress around 0.4GPa to the channel in both longitudinal and transverse directions. That is the tensile-stress induced by the 500°C RTP2improves the 10% ION of NMOS as shown in Fig. 9. It has been reported, the induced stress should be consistent to the piezo-resistance coefficient to benefit different type MOSFET. The prefer stress type for enhancing mobility is shown in Fig.10. As seen, the induced in the developed method is tensile stress, which is consistent to NMOSFET in longitudinal direction but not to PMOSFET, thus improves NMOS only. The induced tensile stress becomes higher as RTP2 temperature is raised to 700 °C; it increases the pressure to the channel up to 1.3GPa (blanket test data, Fig. 5), and recovers the step-height from 18nm (500°C) to 20nm (Fig. 6c). Additionally, at 700°C, the FUSI gate agglomerates and forms voids (Fig. 6c) thus seriously degrading the value of ION. Moreover, based on C/V measurement, Toxinv was reduced by 0.3nm. This is the same as the findings of poly depletion reduction in the conventional FUSI device, and thus evidences the envelope of the FUSI gate with the second CESL fully silicided gate down to the dielectric interface.

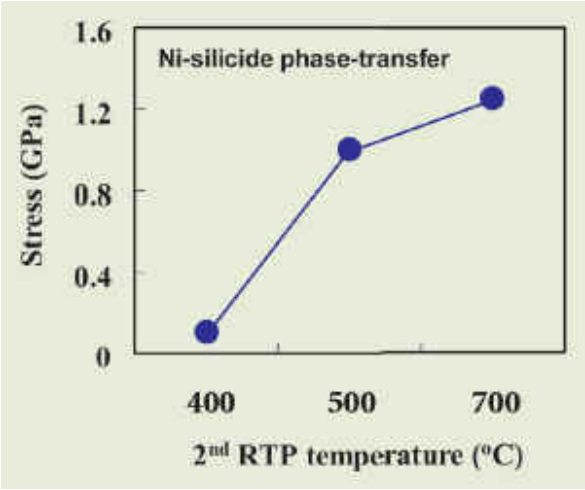


Fig. 5 Ni-silicide phase transform induced stress as a function of FUSI RTP2 temperature.

Fig. 6 TEM cross-sectional micrograph of the FUSI gate: (a) with RTP2 at 500°C, prior to the second CESL deposition, (b) after deposition of the second CESL and RTP2 at 500°C,and (c) after deposition of the second CESL and RTP2 at 700°C. 20 30 40 50 60 2θ (degress)

In summary, manipulating tensile stress by means of phase transform and volume change of a CESL-enveloped FUSI gate after FUSI RTP2 has been studied in detail and demonstrated that the method indeed improves CMOS performance significantly. For example, under FUSI RTP2 at 500°C, the confined NixSi FUSI reduces the step height by 60% and transforms the phase from NixSi to NixSiy mixture phase thus generates obvious tensile stress in the channel for 10% improvement of NMOS ION. Best of all, this novel strain engineering only exchanges the sequence of FUSI RTP2 and the second CESL processes without adding any extra process or mask steps. Particularly the technology does not affect the function of reducing gate depletion. Therefore, the developed FUSI strain engineering is very promising for future high-performance logic CMOS technology.

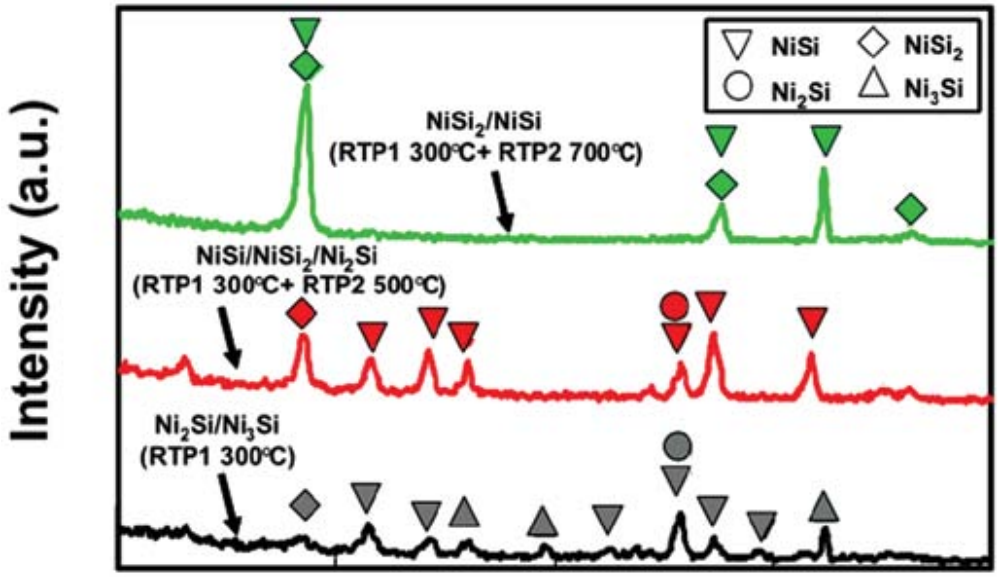


Fig. 7 XRD spectrum on blanket wafers, with stack of Ni/poly-Si/gate dielectric/Si, showing phase transform of the enveloped FUSI after 300°C to 700°C RTP2. The Ni to Si thickness ratio is 0.6.

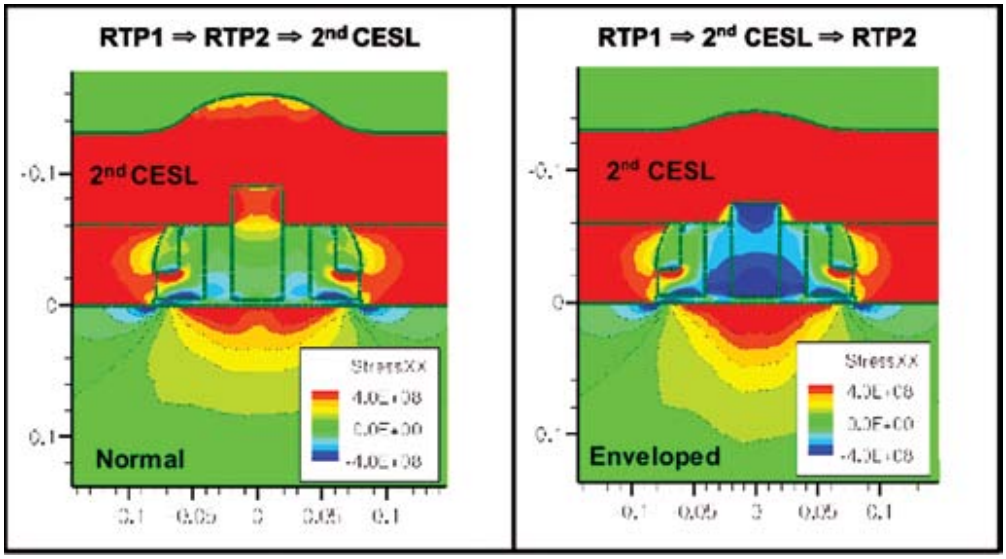


Fig. 8 Simulation showing that enveloped FUSI exhibits higher tensile stress in the longitudinal direction.

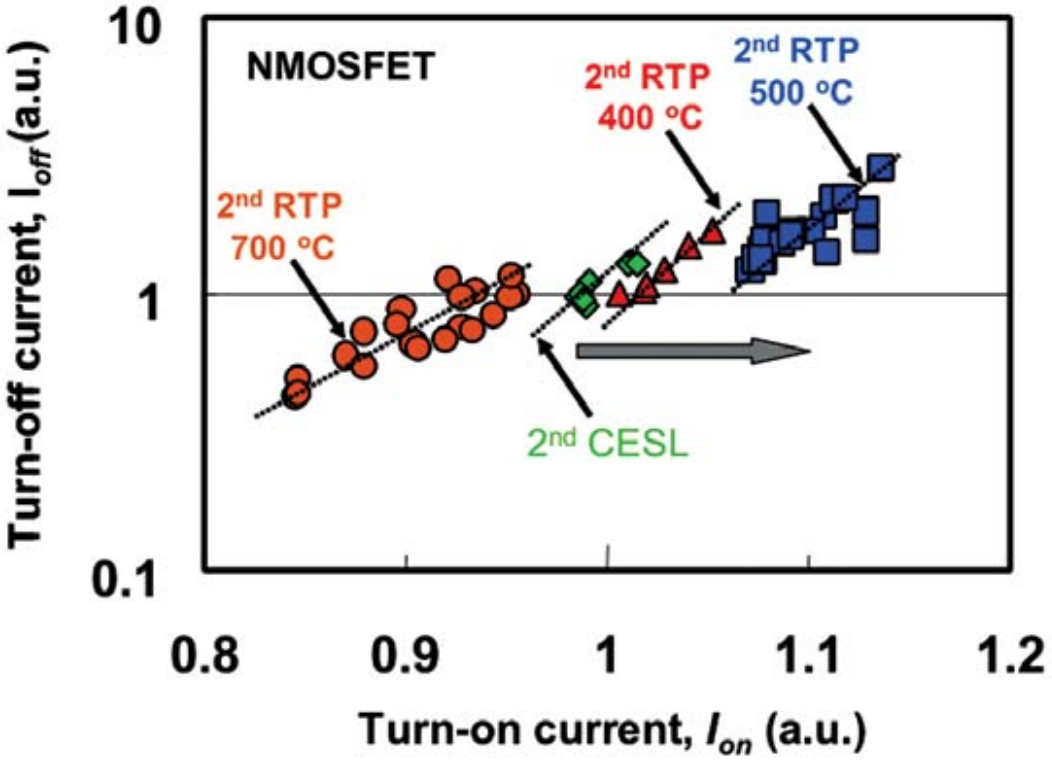
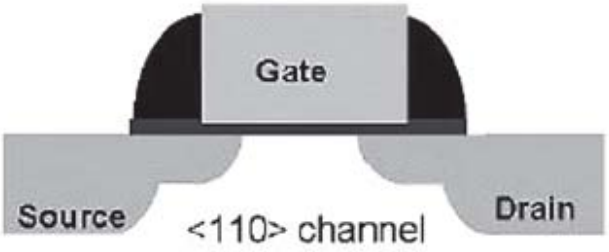


Fig. 9 ION vs. IOFF of NMOS with enveloped FUSI gate as a function of RTP2 temperature.



Type of Stress Needed for Enhanced Mobility

Direction	NMOS	PMOS
Longitudinal	Tension +++	Compression ++++
Transverse	Tension ++	Tension +++
Out-of-plane	Compression ++++	Tension +

資料來源: ***S. E. Thompson et al., "A logic nanotechnology featuring strained-silicon," IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. 25, pp. 191 - 193, April 2004.***

Fig. 10 From piezoresistance, the effect of various stress on electron and hole mobility.